

FIG. 1

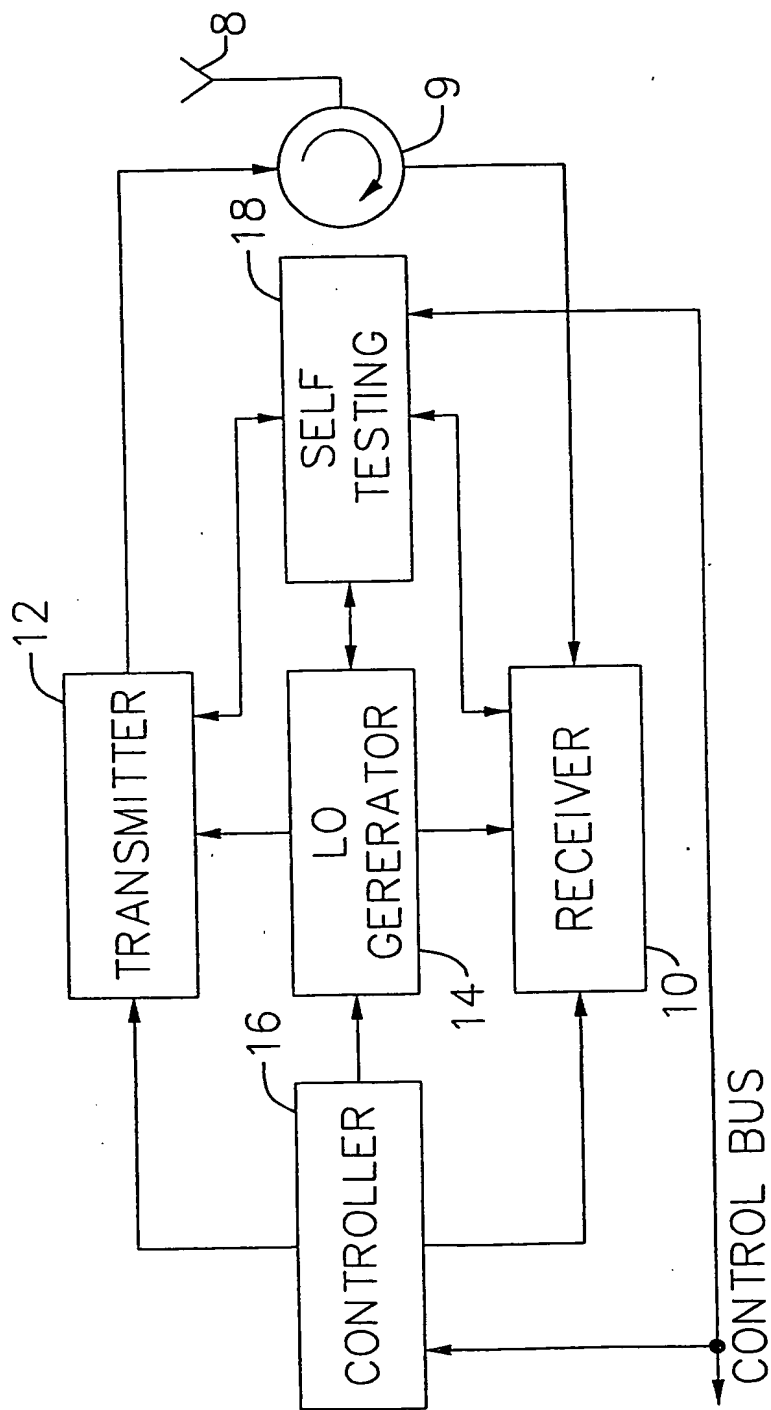


FIG. 2

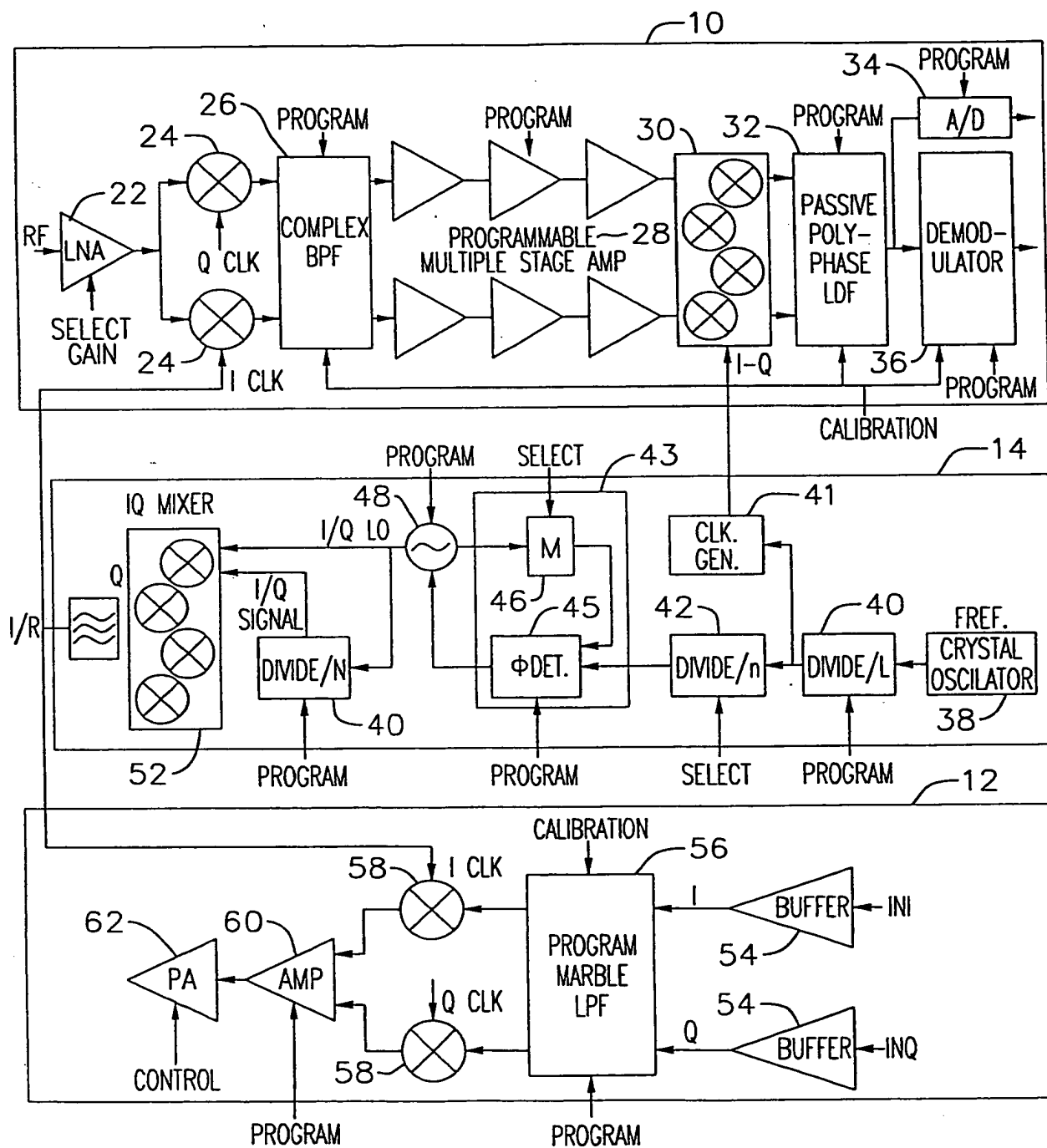


FIG. 3

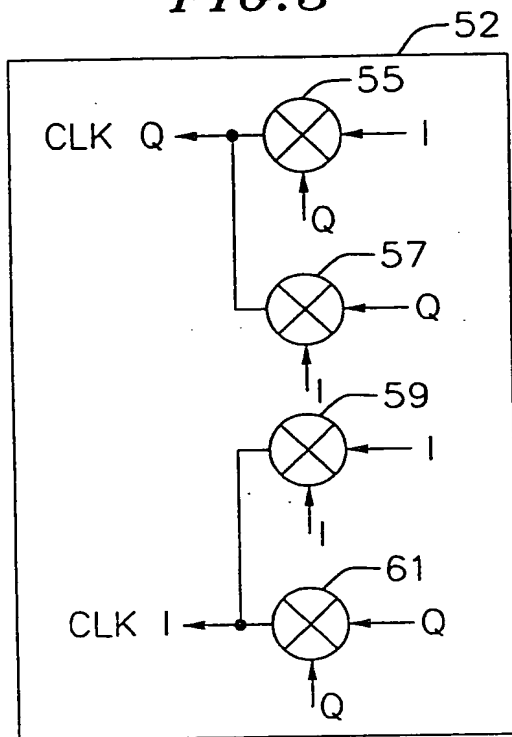
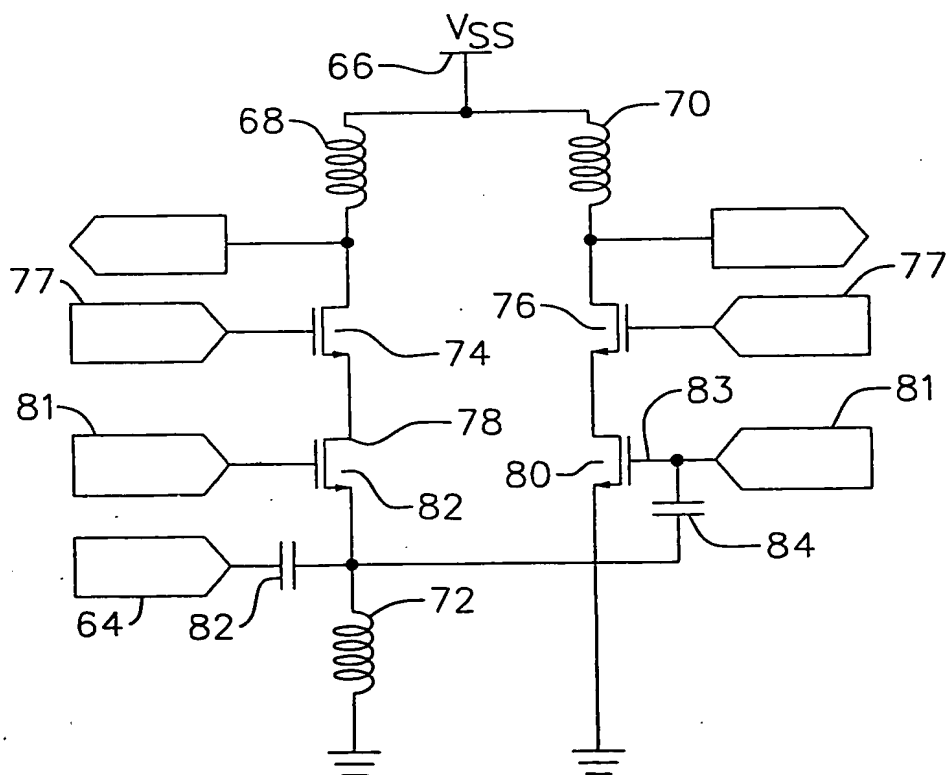


FIG. 4



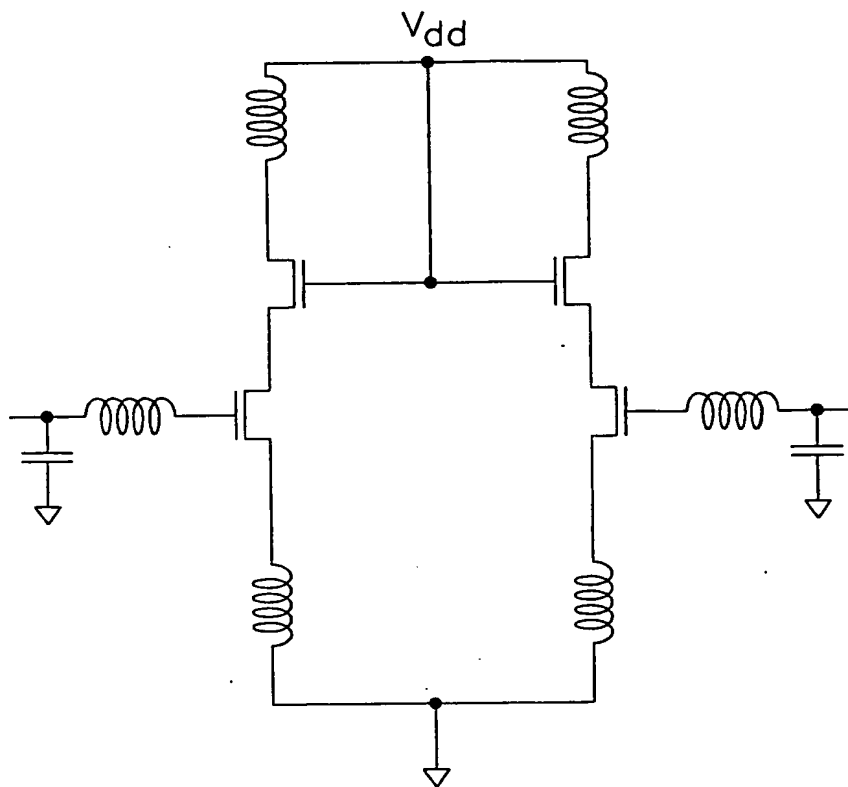
*FIG. 4(a)*



FIG. 5

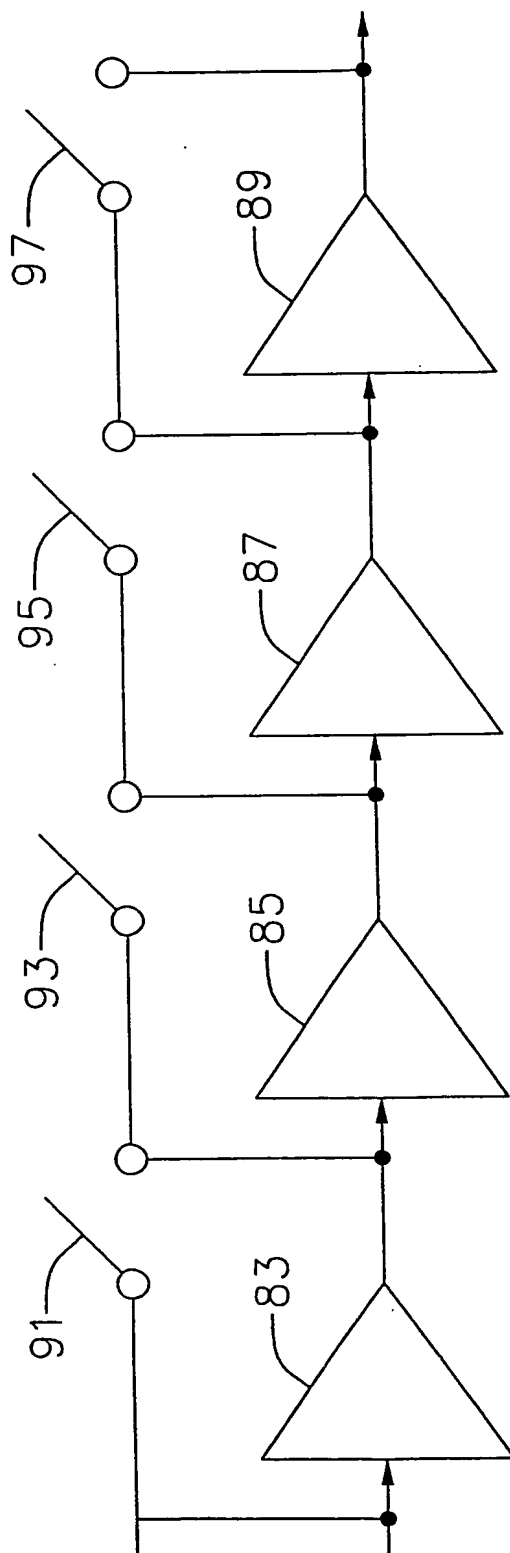


FIG. 6

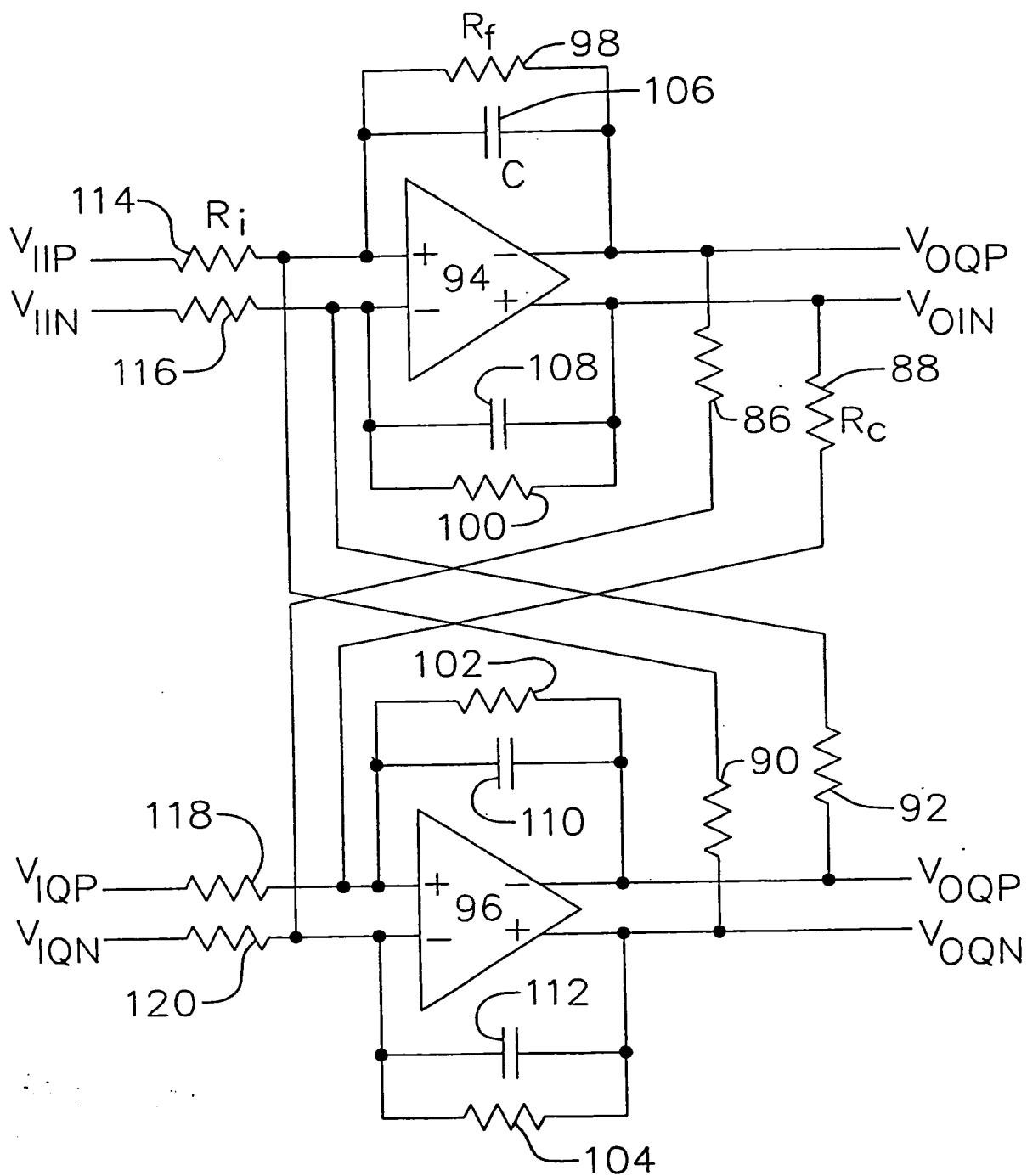


FIG. 7

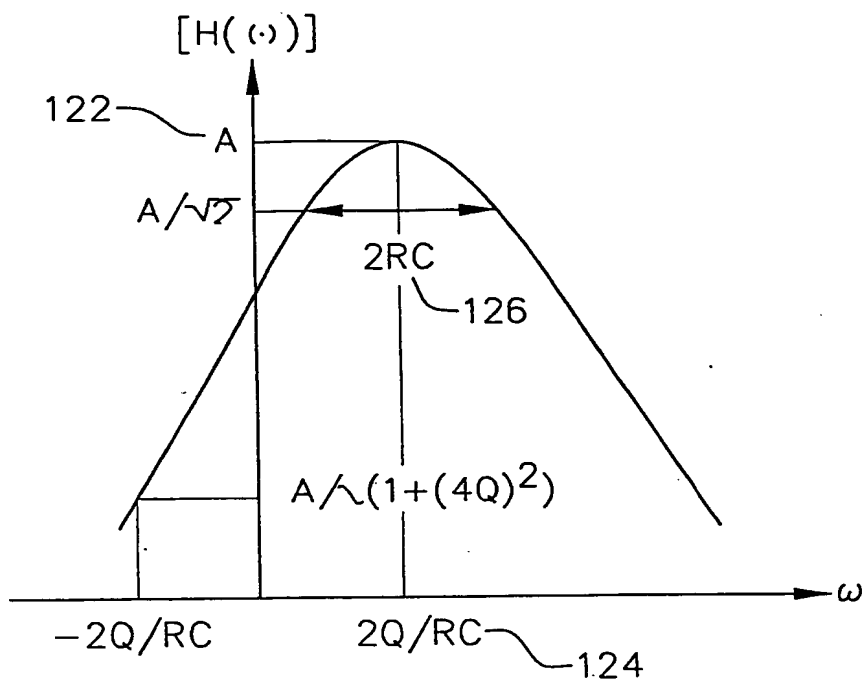


FIG. 8

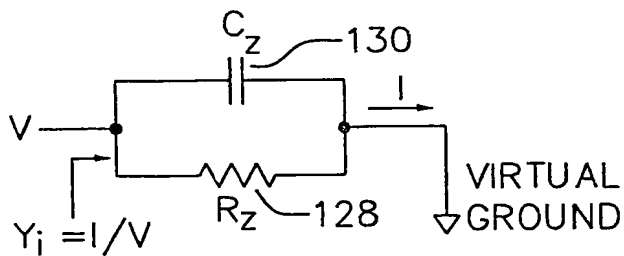


FIG. 9

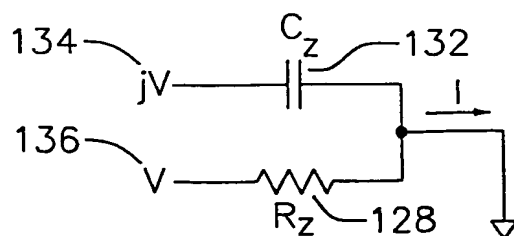


FIG. 10

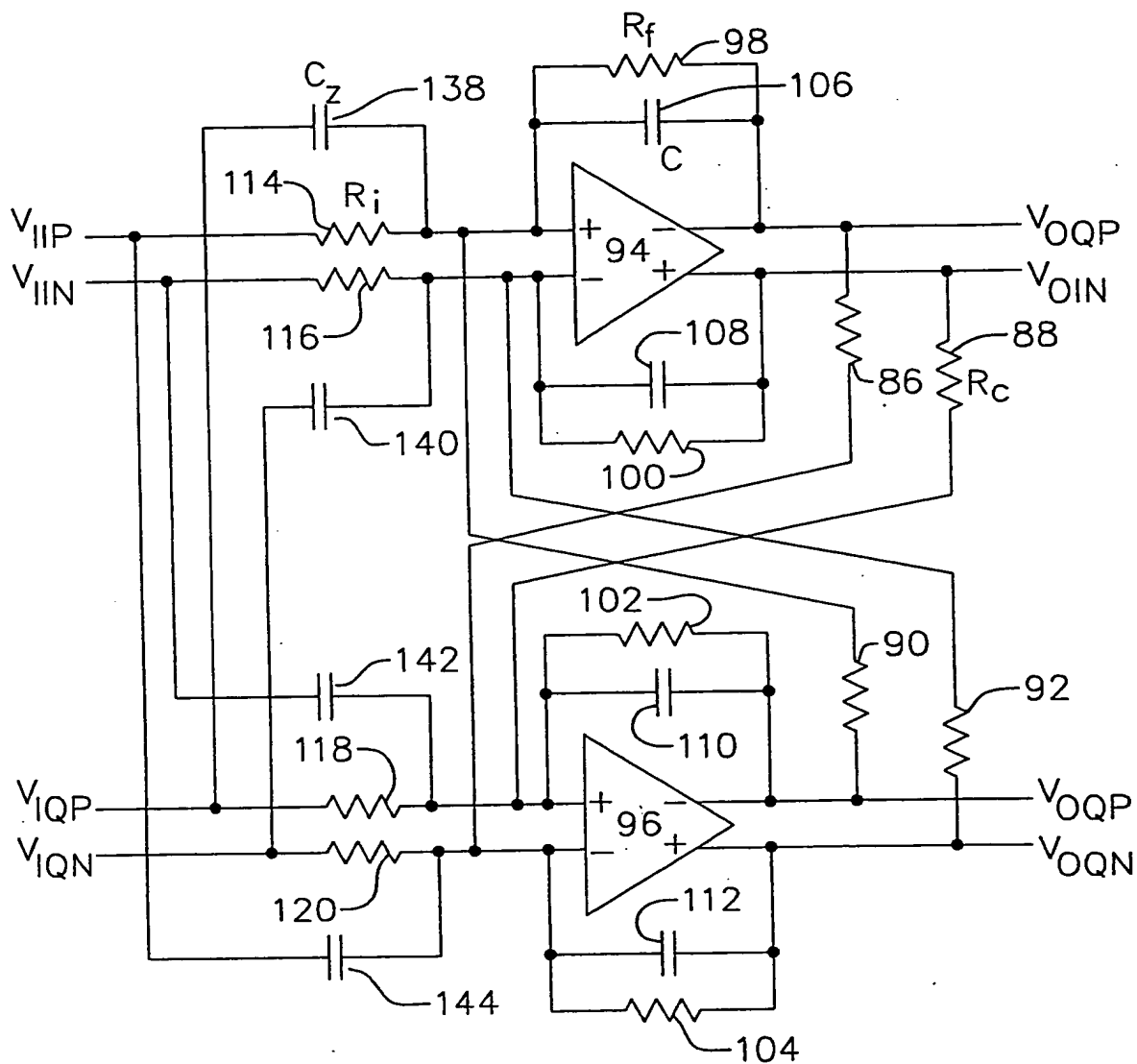




FIG. 11

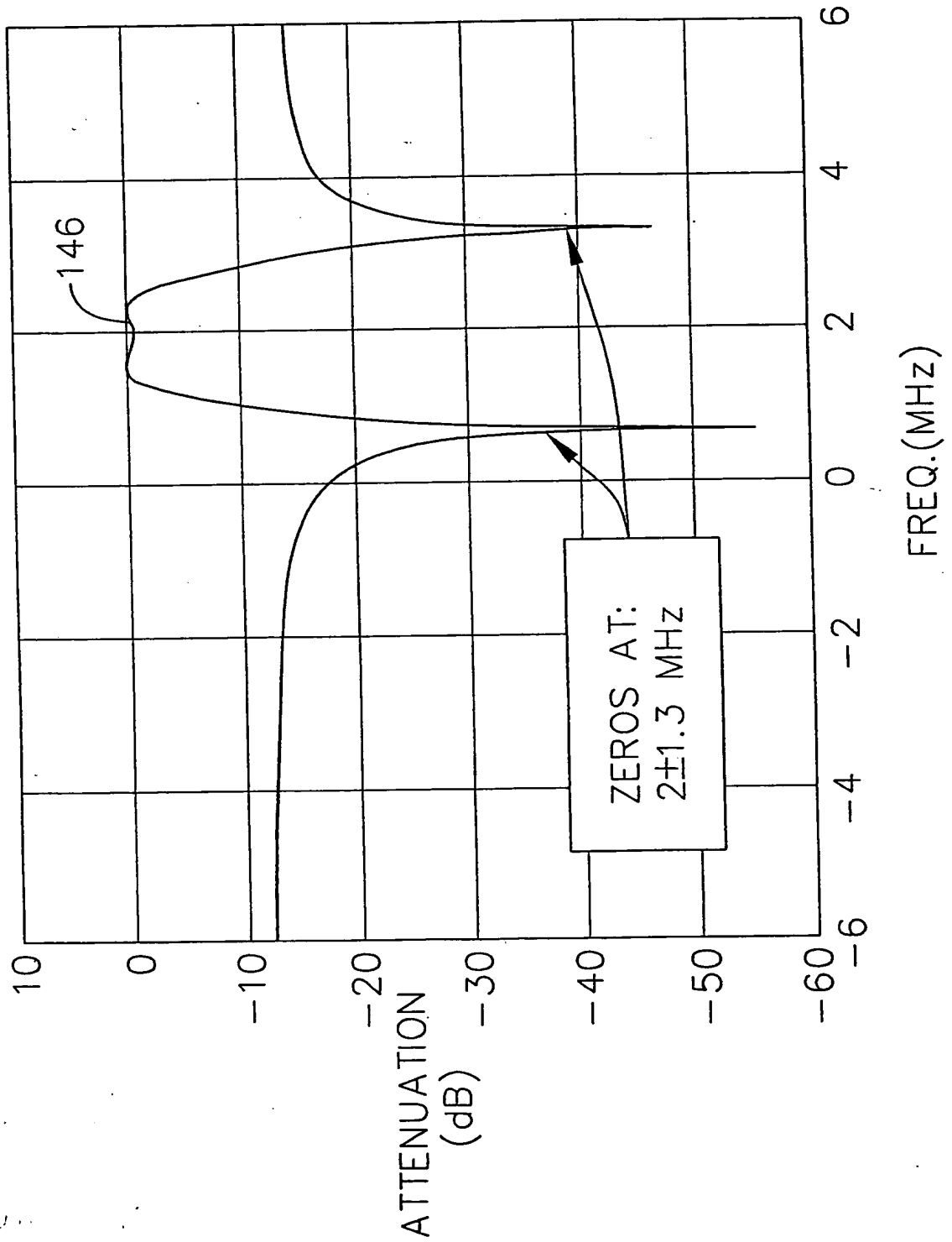




FIG. 12a

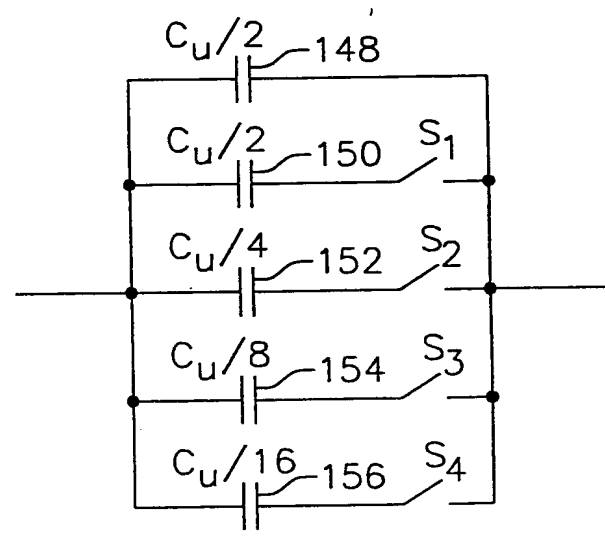


FIG. 12b

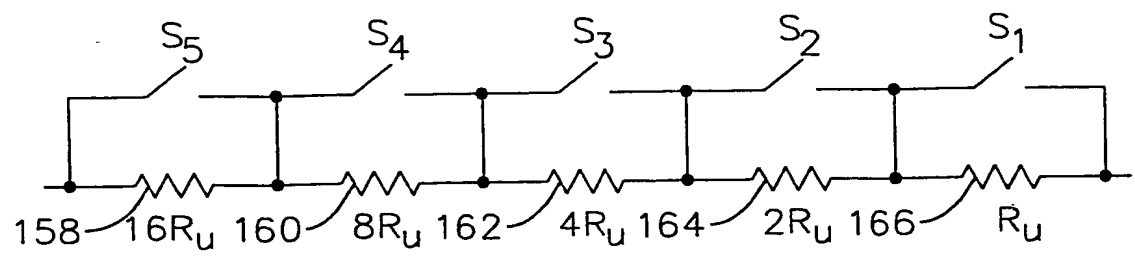


FIG. 13

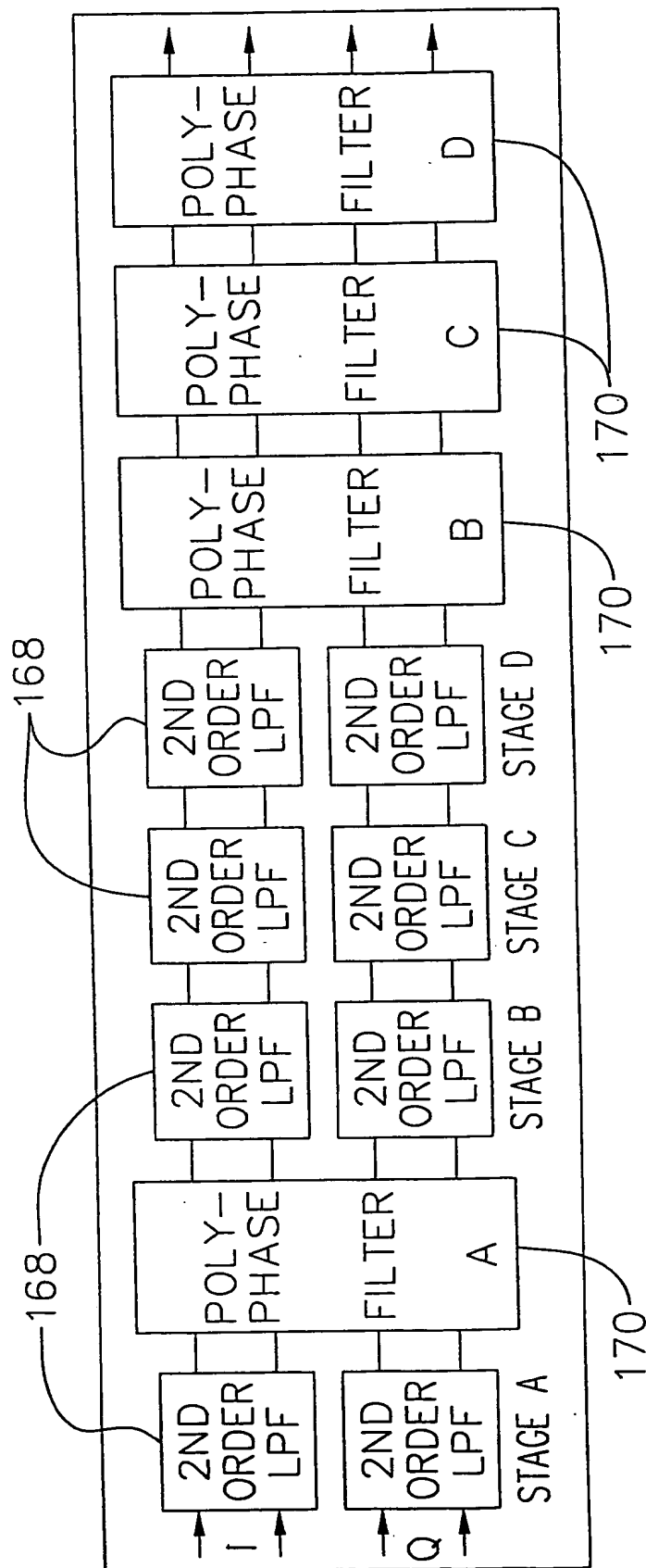
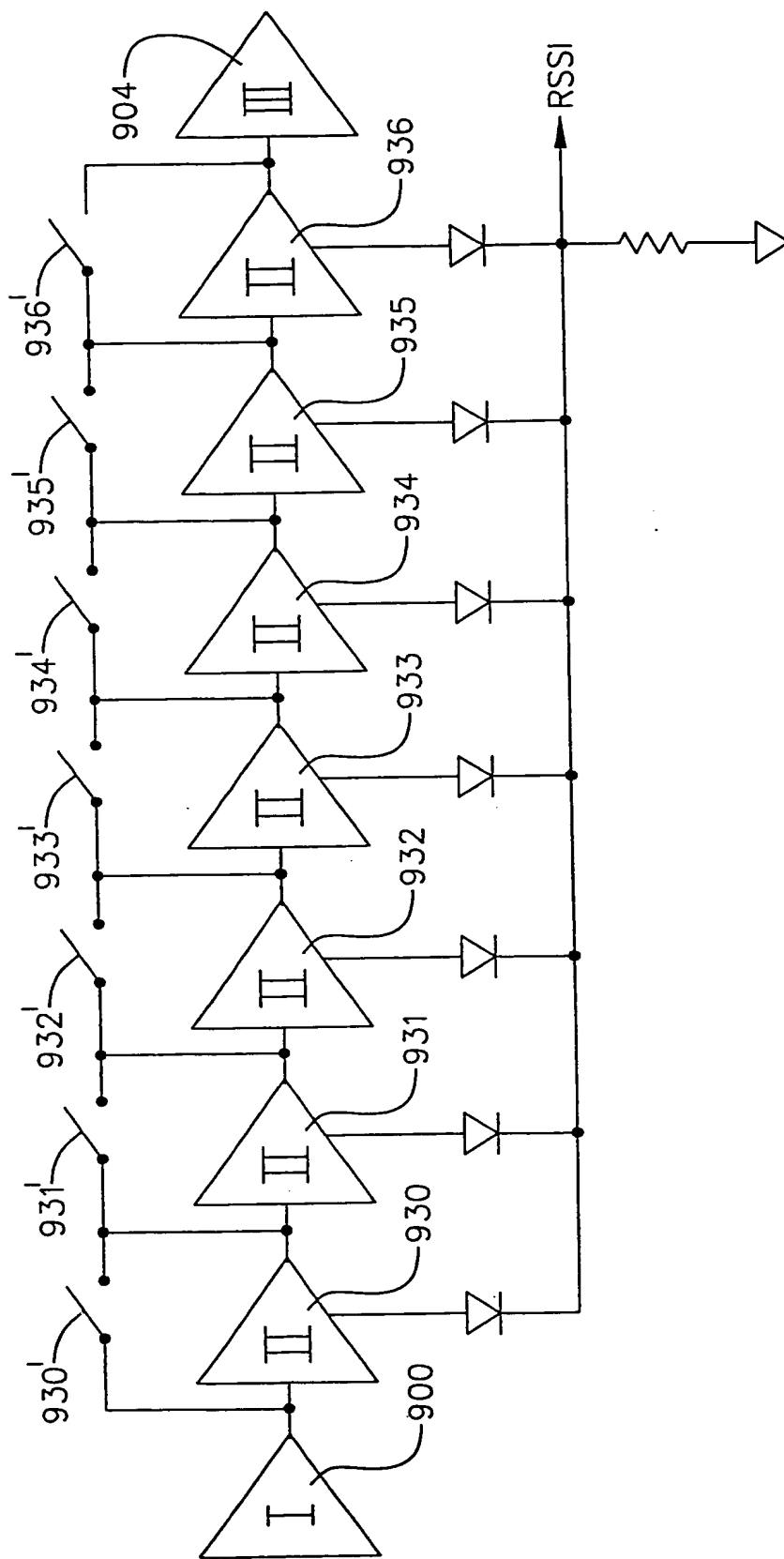


FIG. 14



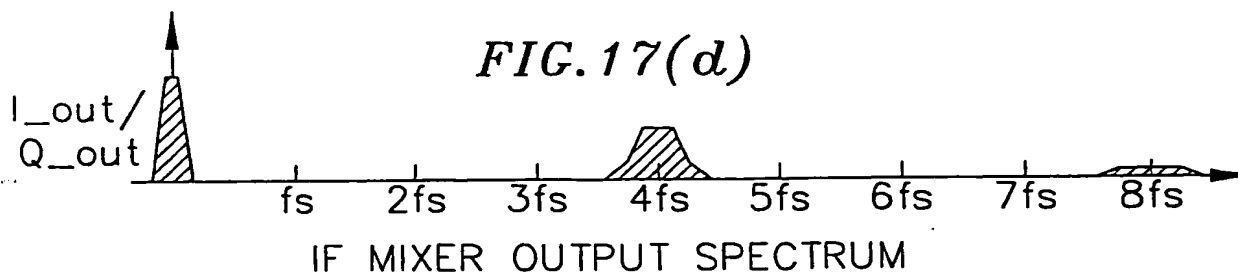
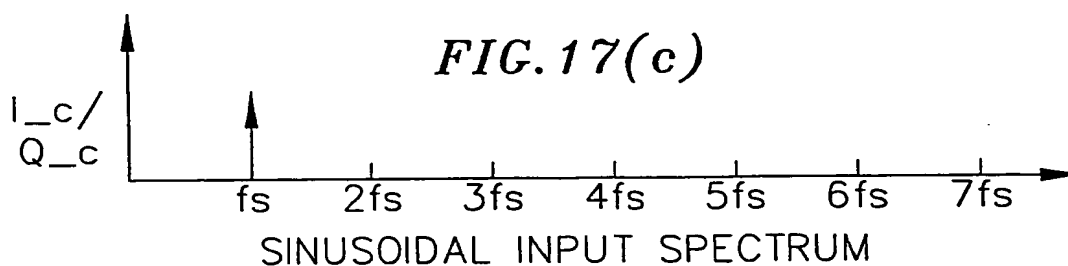
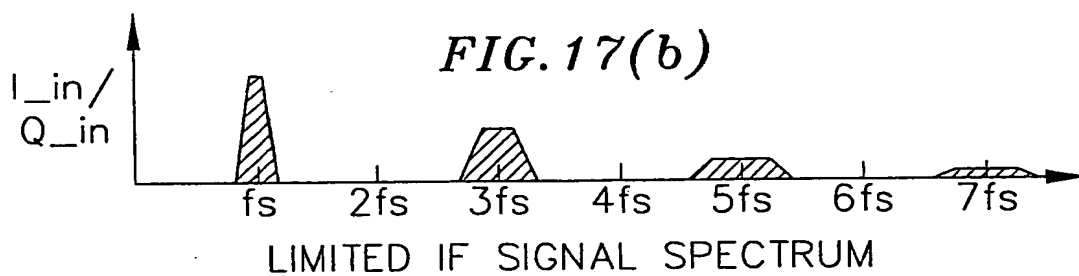
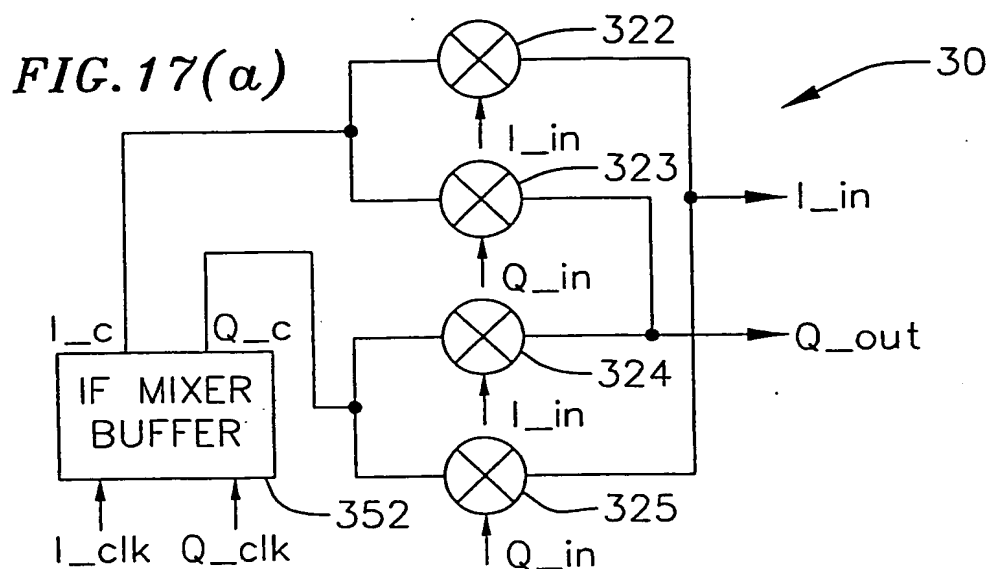


FIG. 18

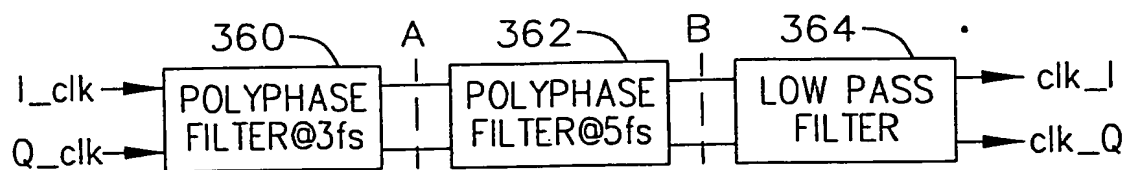


FIG. 19(a)

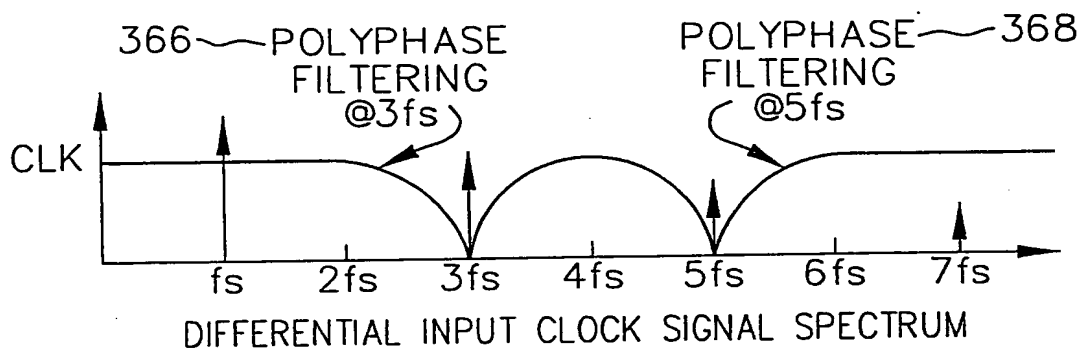


FIG. 19(b)

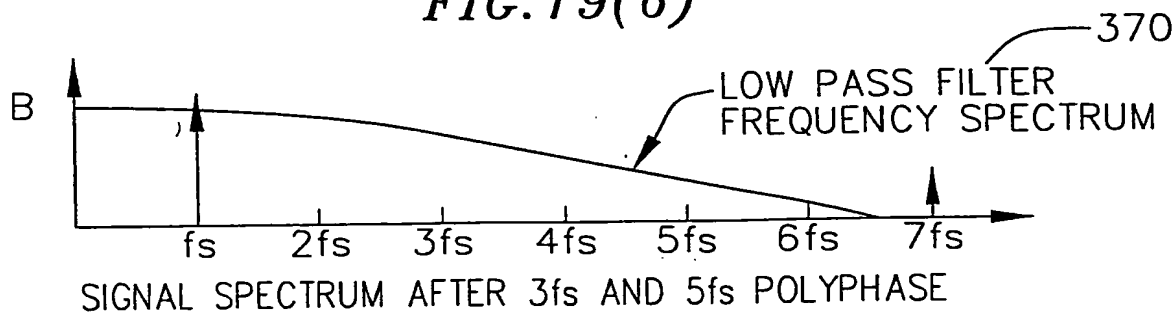


FIG. 19(c)

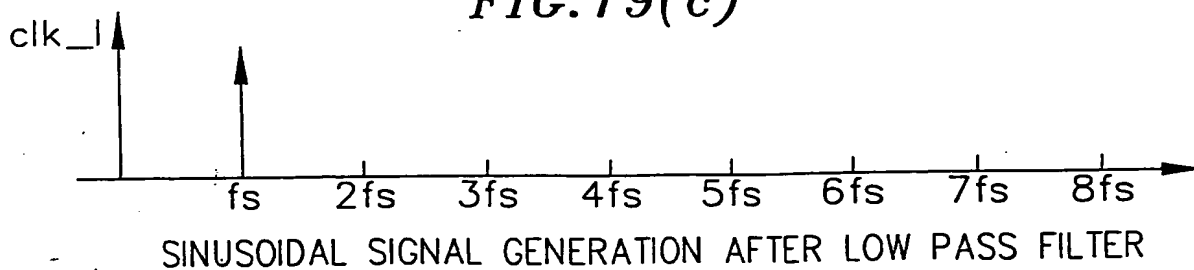
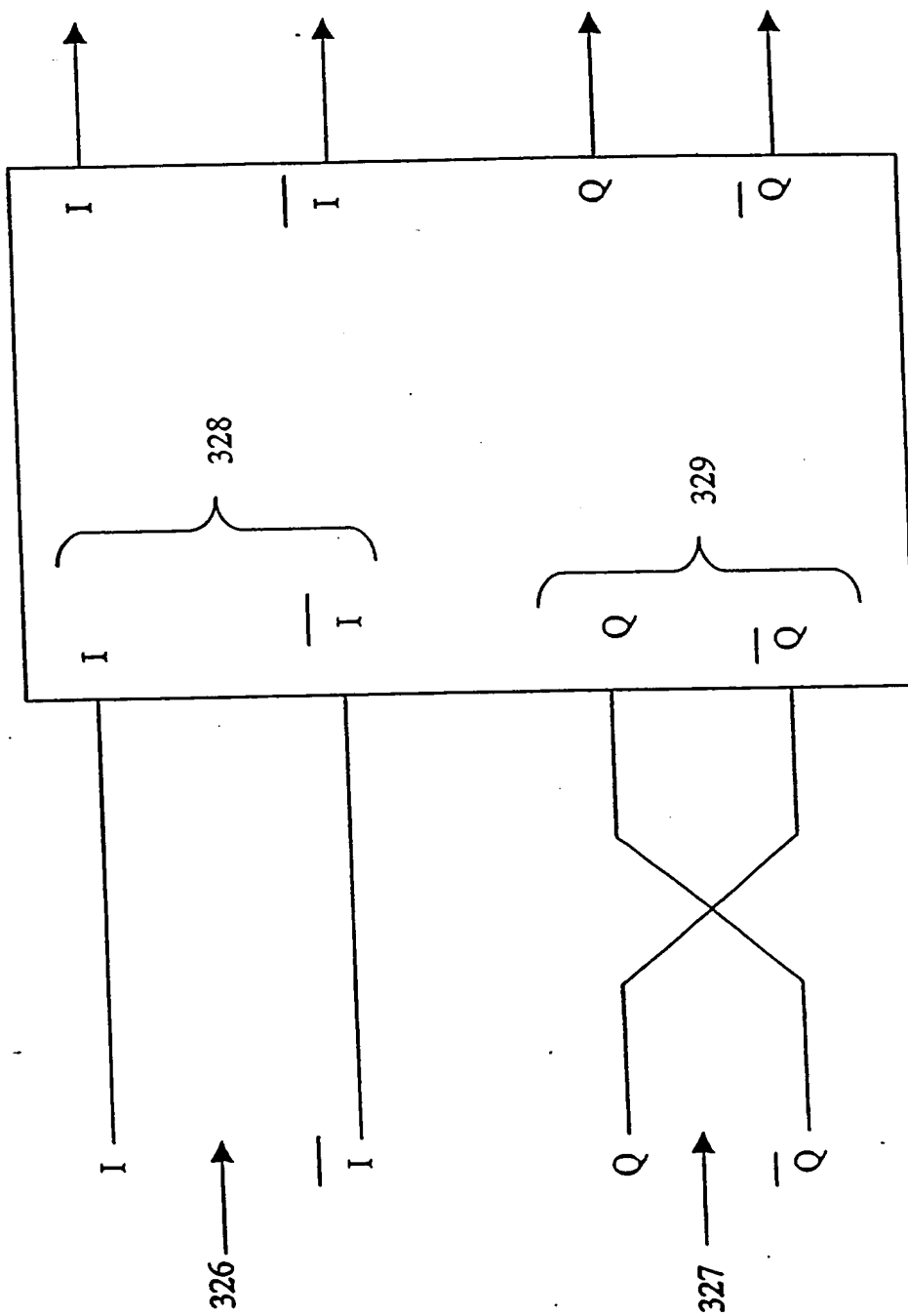




FIG. 19d



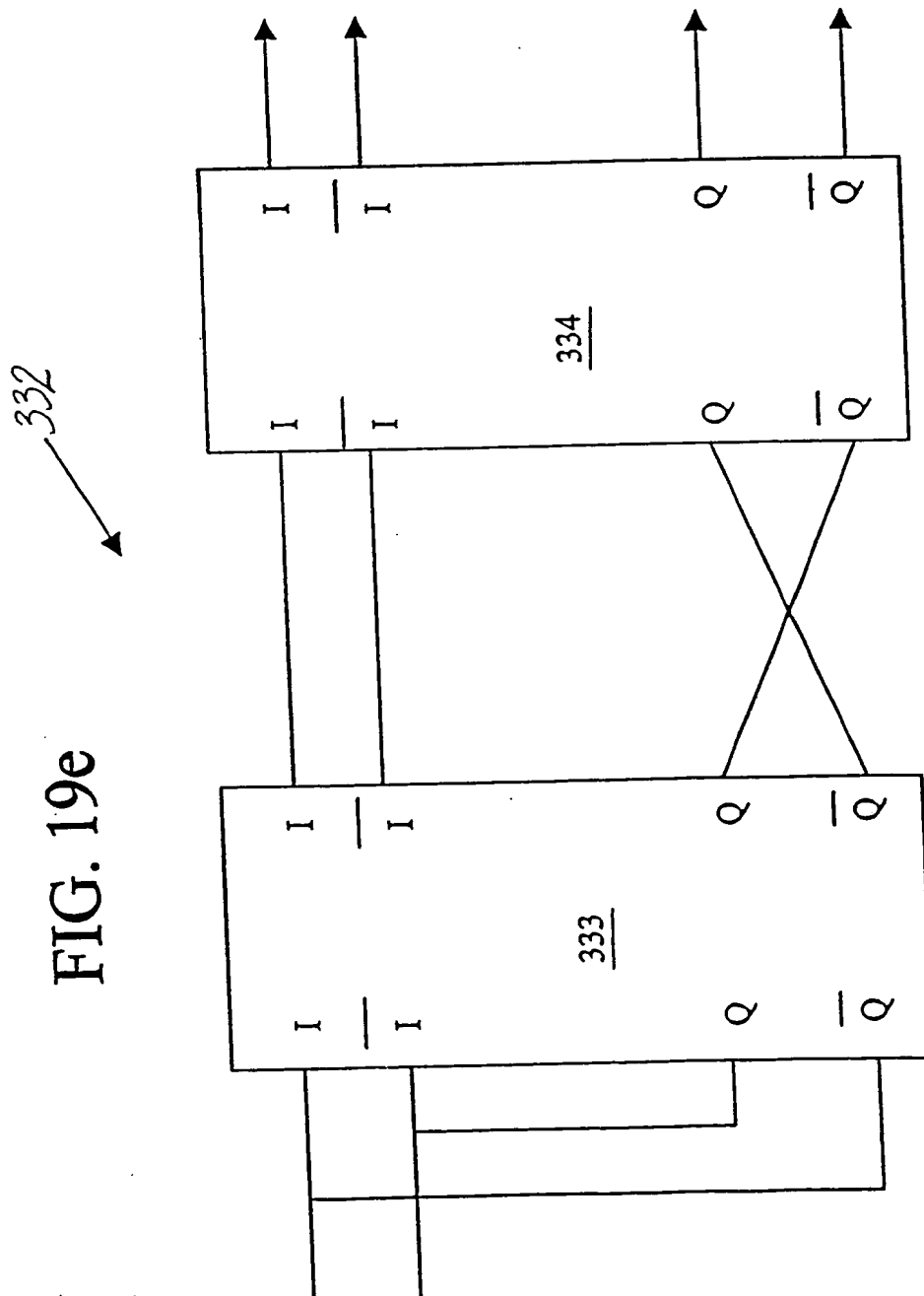


FIG. 19f

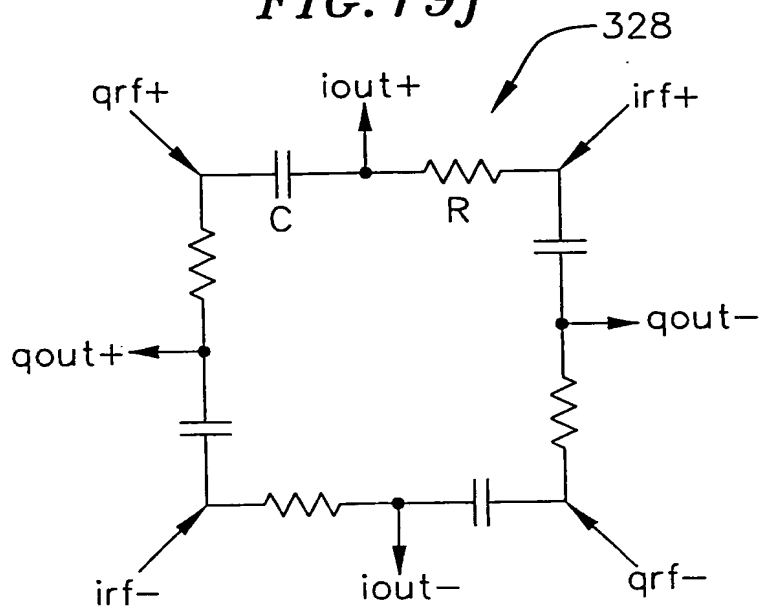
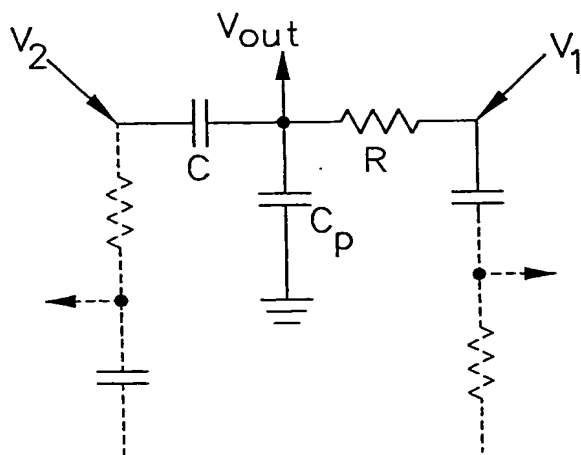


FIG. 19g



$$\omega_p = \frac{1}{R(C_p + C)}$$

$$\omega_o = \frac{1}{RC}$$

$$V_{out} = \frac{V_1}{R(C_p + C)s + 1} + \frac{V_2 RCs}{R(C_p + C)s + 1}$$

FIG.20(a)

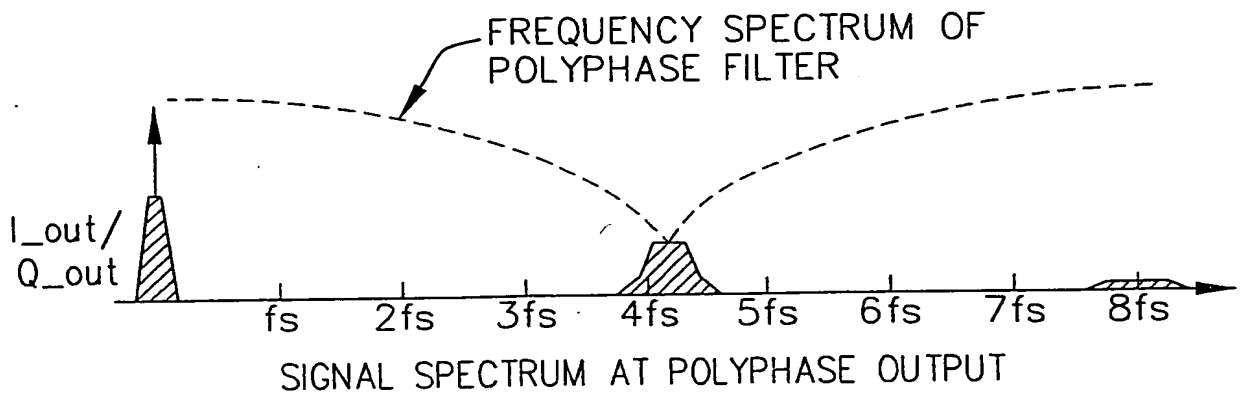


FIG.20(b)

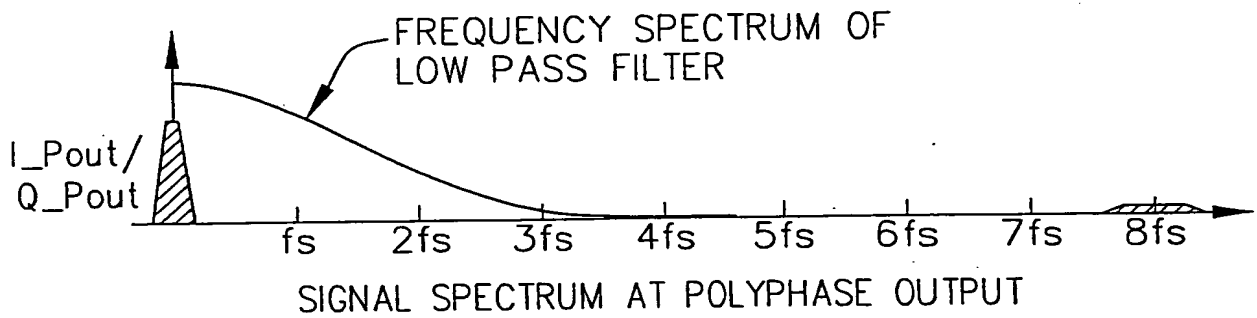


FIG.20(c)

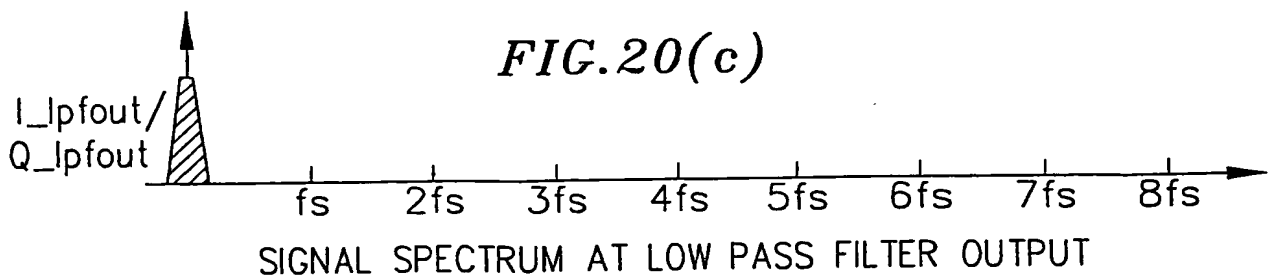


FIG. 21

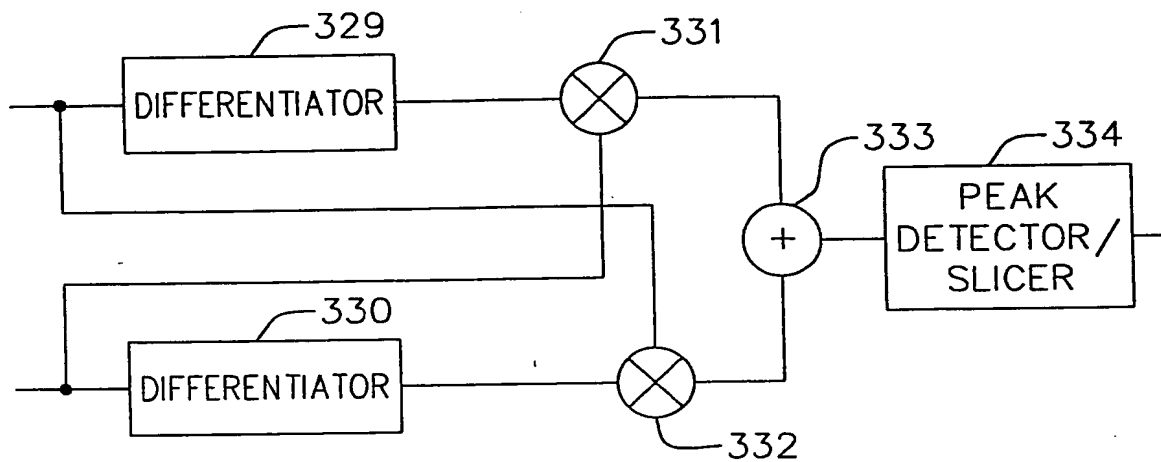
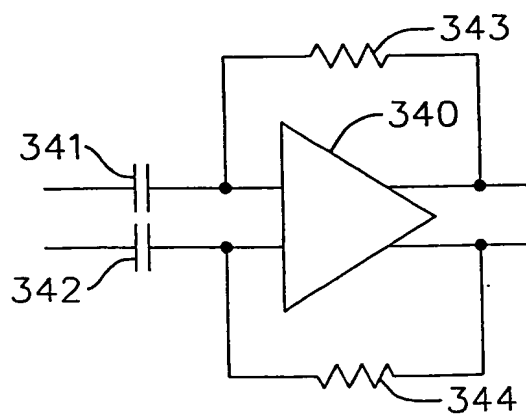


FIG. 22



The circuit diagram shows two buffers, BUFFER 1 (334) and BUFFER 2 (335), each with two outputs: C and \overline{C} for BUFFER 1, and D and \overline{D} for BUFFER 2. BUFFER 1's output C is connected to the gate of PMOS transistor 344, and \overline{C} is connected to the gate of NMOS transistor 346. BUFFER 2's output D is connected to the gate of PMOS transistor 336, and \overline{D} is connected to the gate of NMOS transistor 338. The drains of transistors 344 and 346 are connected to the gates of transistors 348 and 350. The drains of transistors 348 and 350 are connected to the gates of transistors 344 and 346, respectively, forming two inverters. The sources of all transistors are connected to ground. The outputs of the inverters are labeled OUTPUT. Pull-up resistors 340 and 342 are connected between the VDD supply and the OUTPUT nodes.

The circuit diagram shows a differential peak detector. It consists of two input lines at the top. The first input line is connected to the top input of a first peak detector (labeled 346) and the top input of a second peak detector (labeled 347). The second input line is connected to the top input of the first peak detector (346) and the top input of the second peak detector (347). The output of the first peak detector (346) is connected to a resistor (labeled 348). The output of the second peak detector (347) is connected to a resistor (labeled 349). The other ends of resistors 348 and 349 are connected to a common node. This common node is connected to the non-inverting input of a differential amplifier (labeled 345). The inverting input of the differential amplifier (345) is connected to the top input line. The output of the differential amplifier (345) is connected to a first inverter (labeled 350). The output of the first inverter (350) is connected to a second inverter (labeled 350). The output of the second inverter (350) is connected to the top input line.

FIG. 25

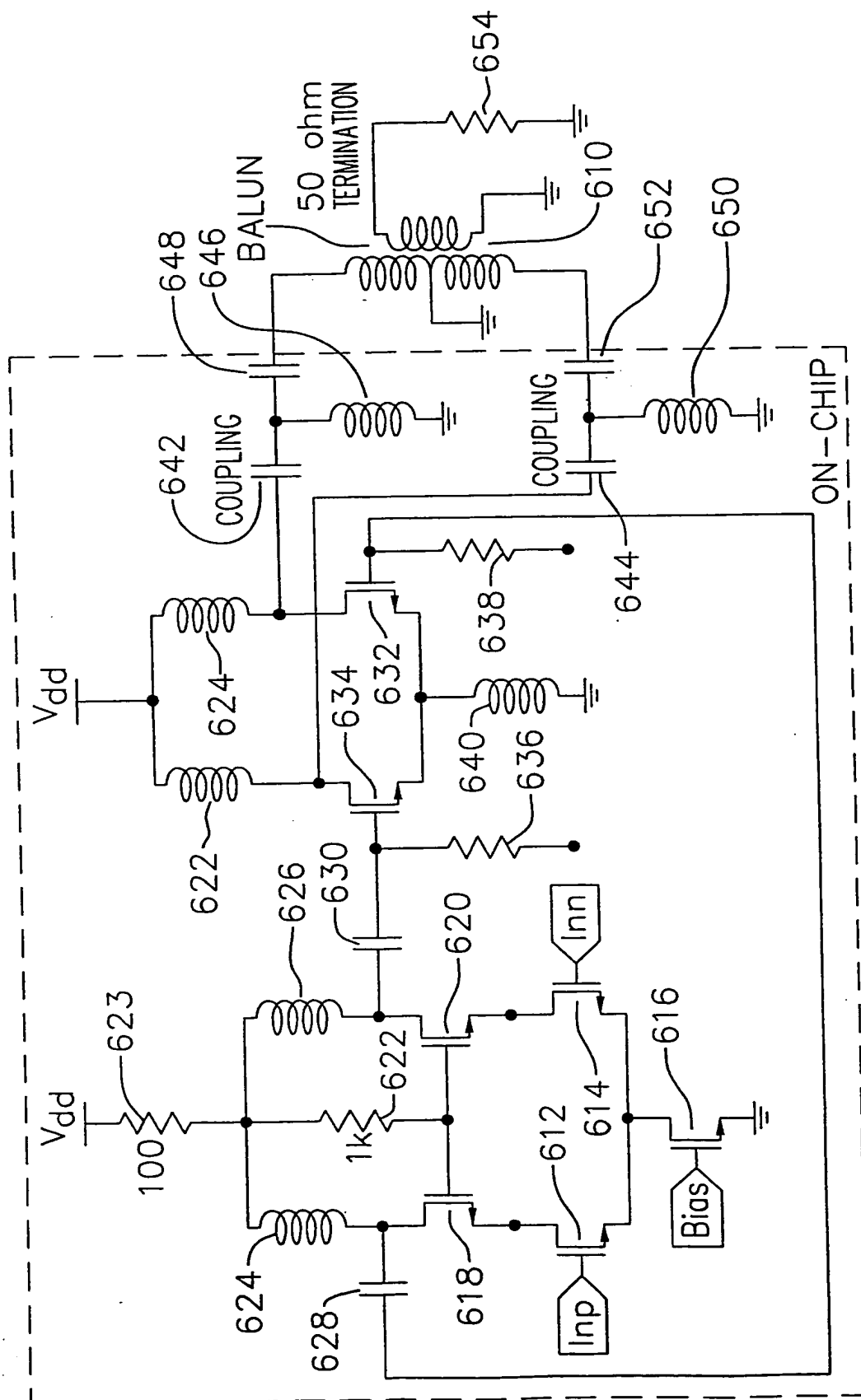


FIG. 26a

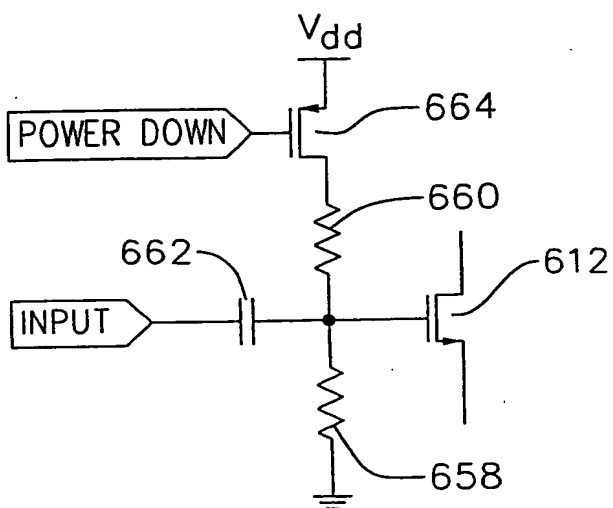


FIG. 26b

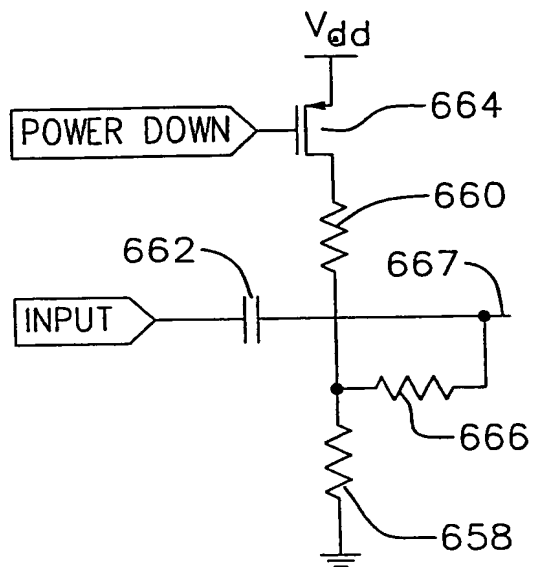


FIG. 27

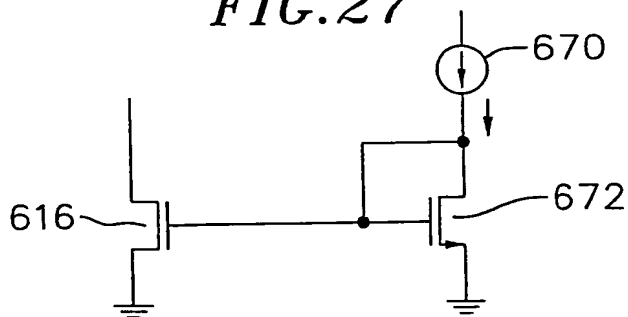


FIG. 28

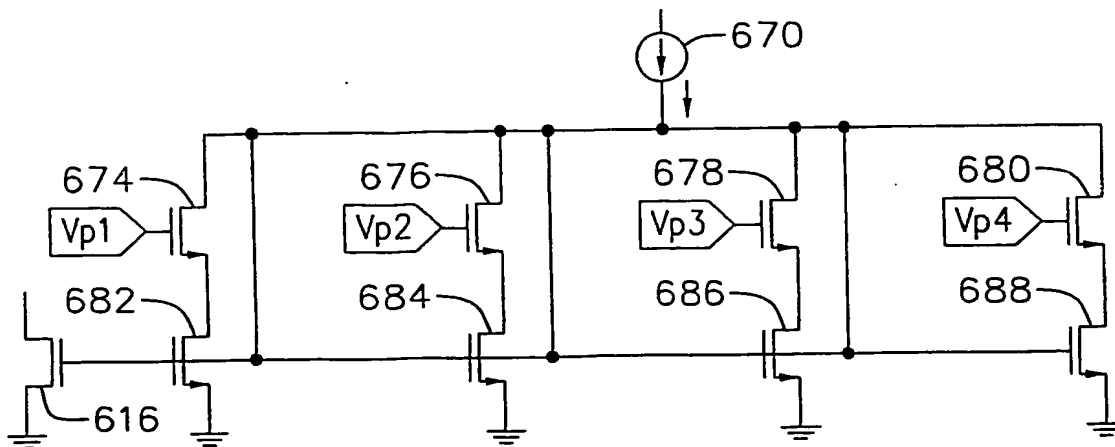


FIG. 29

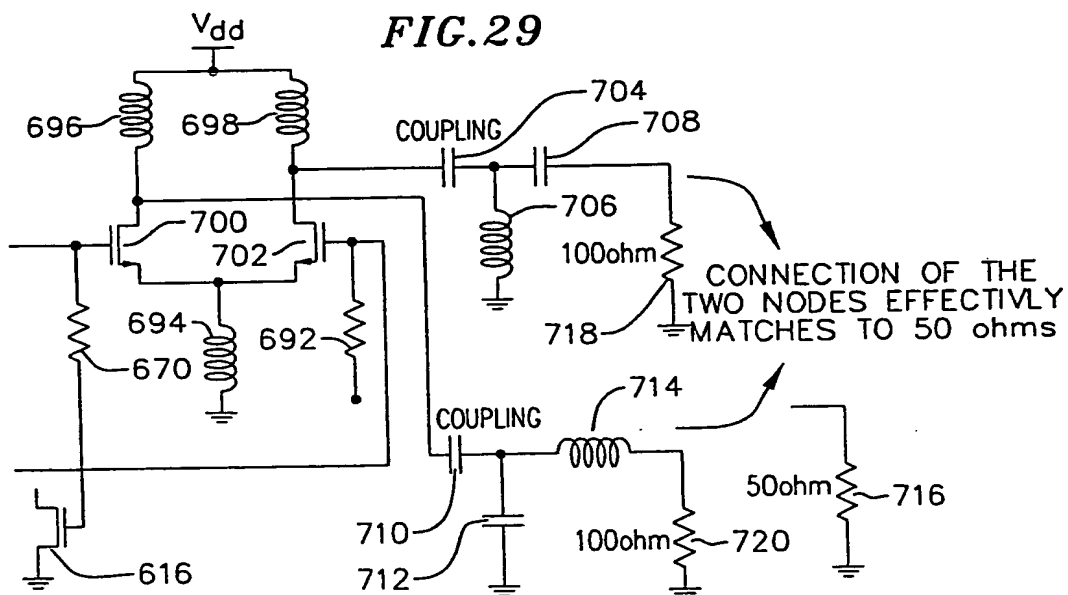
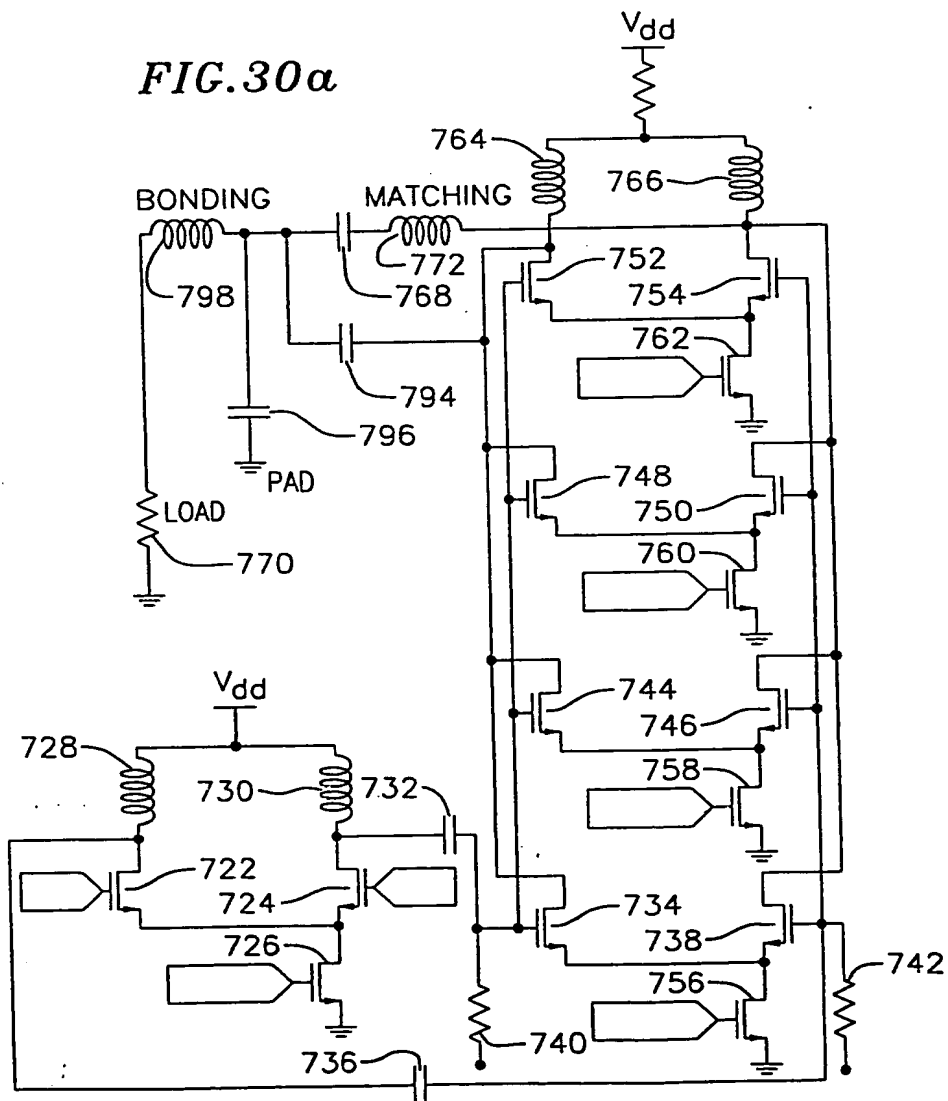


FIG. 30a



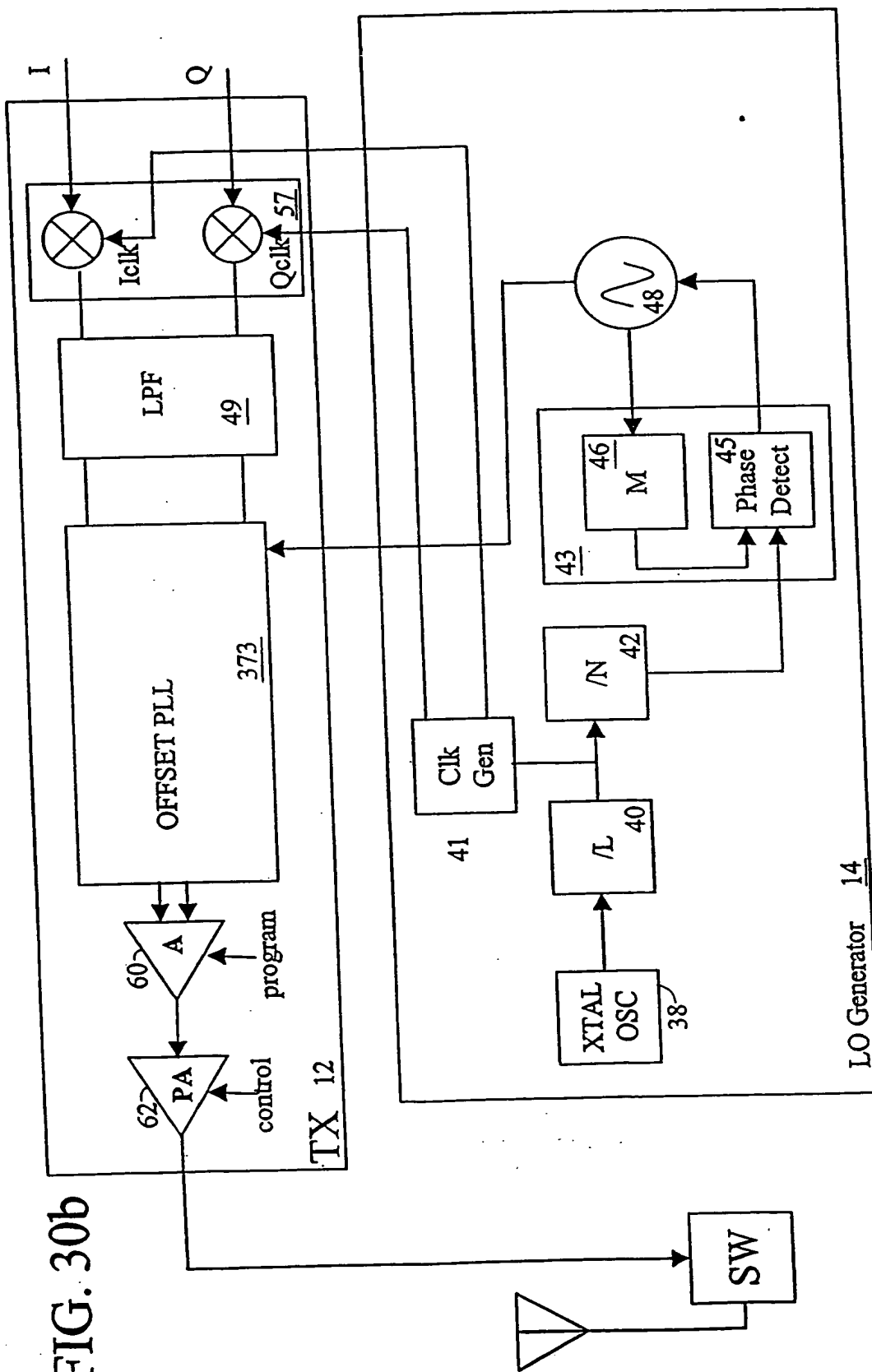


FIG. 30b

FIG. 30c

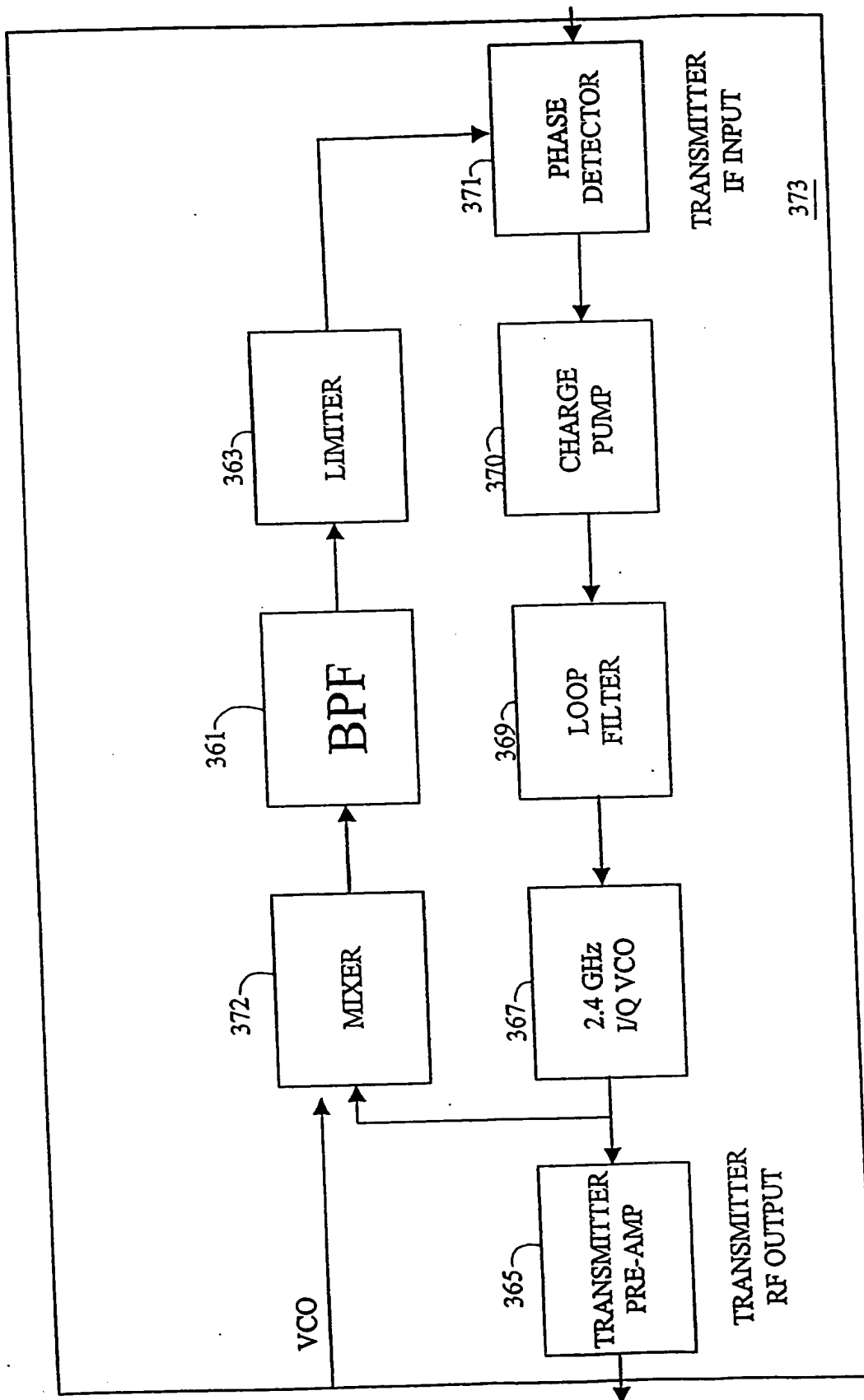
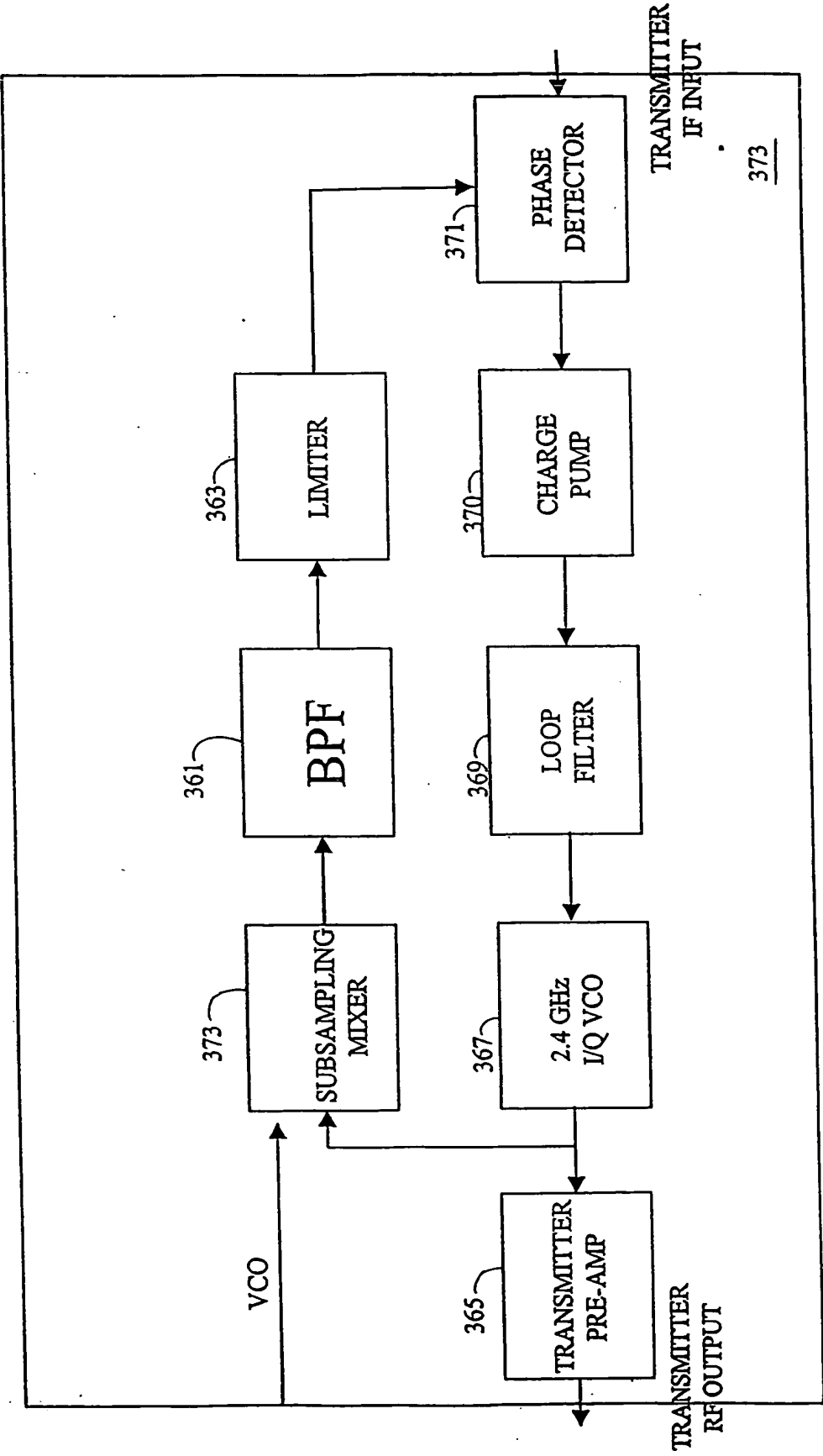
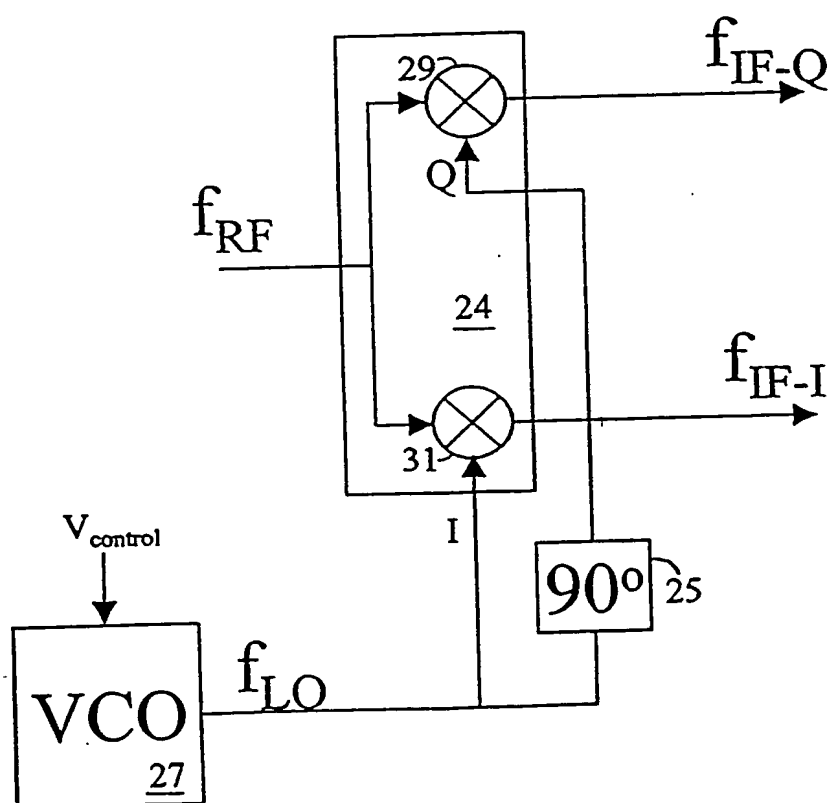
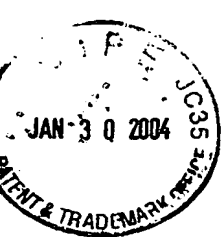




FIG. 30d



*Fig. 30e*



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Fig. 30f

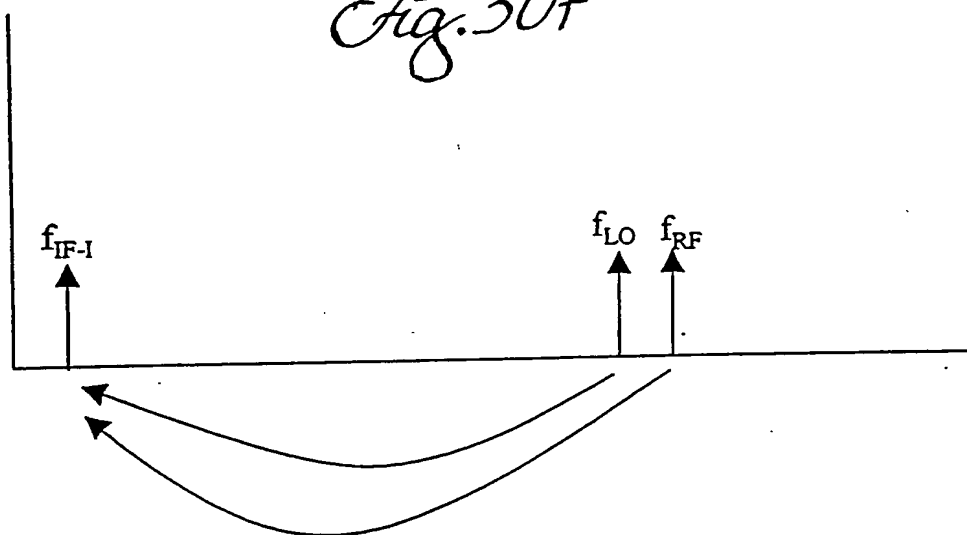
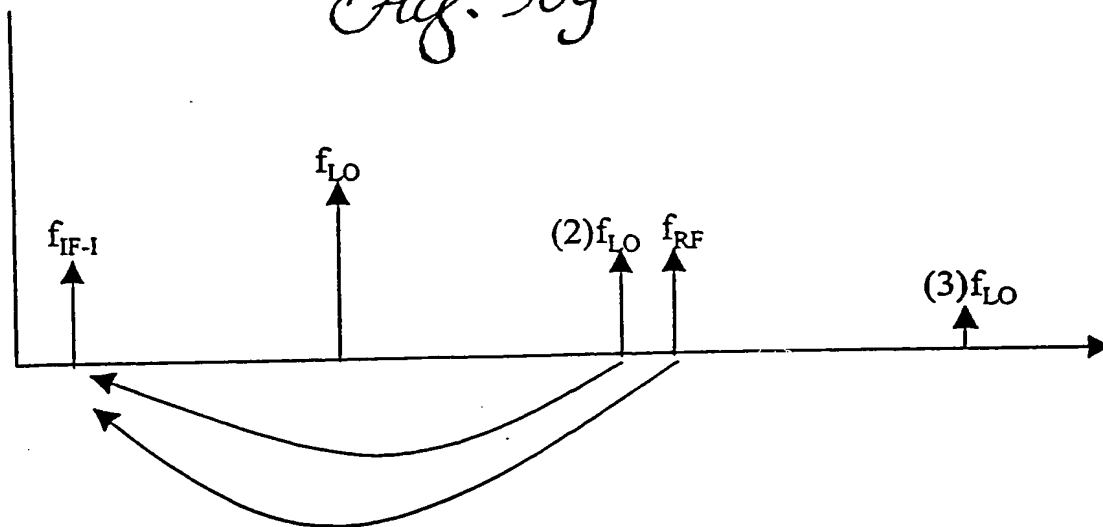


Fig. 30g



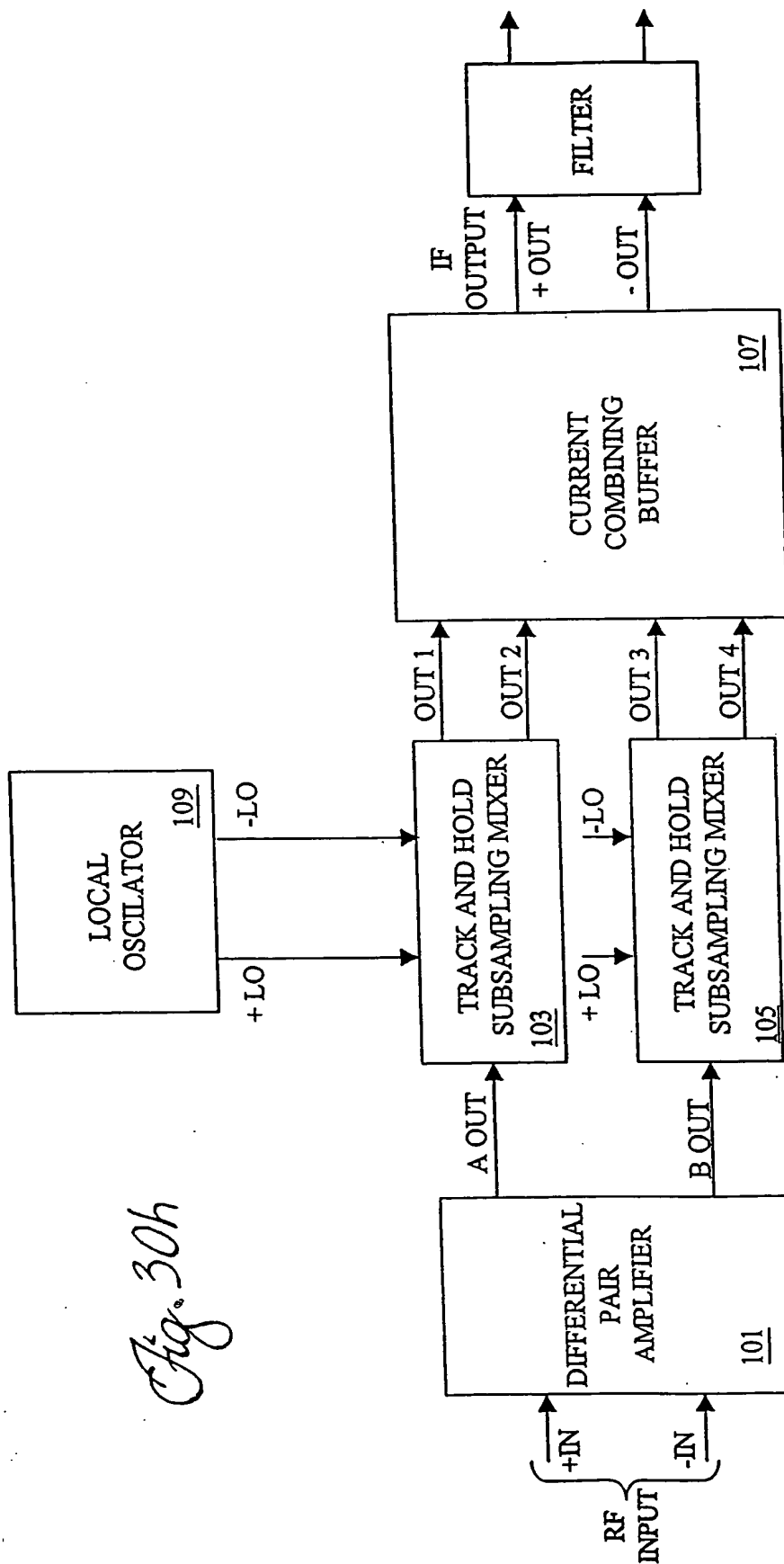


Fig. 30i



Fig. 30j

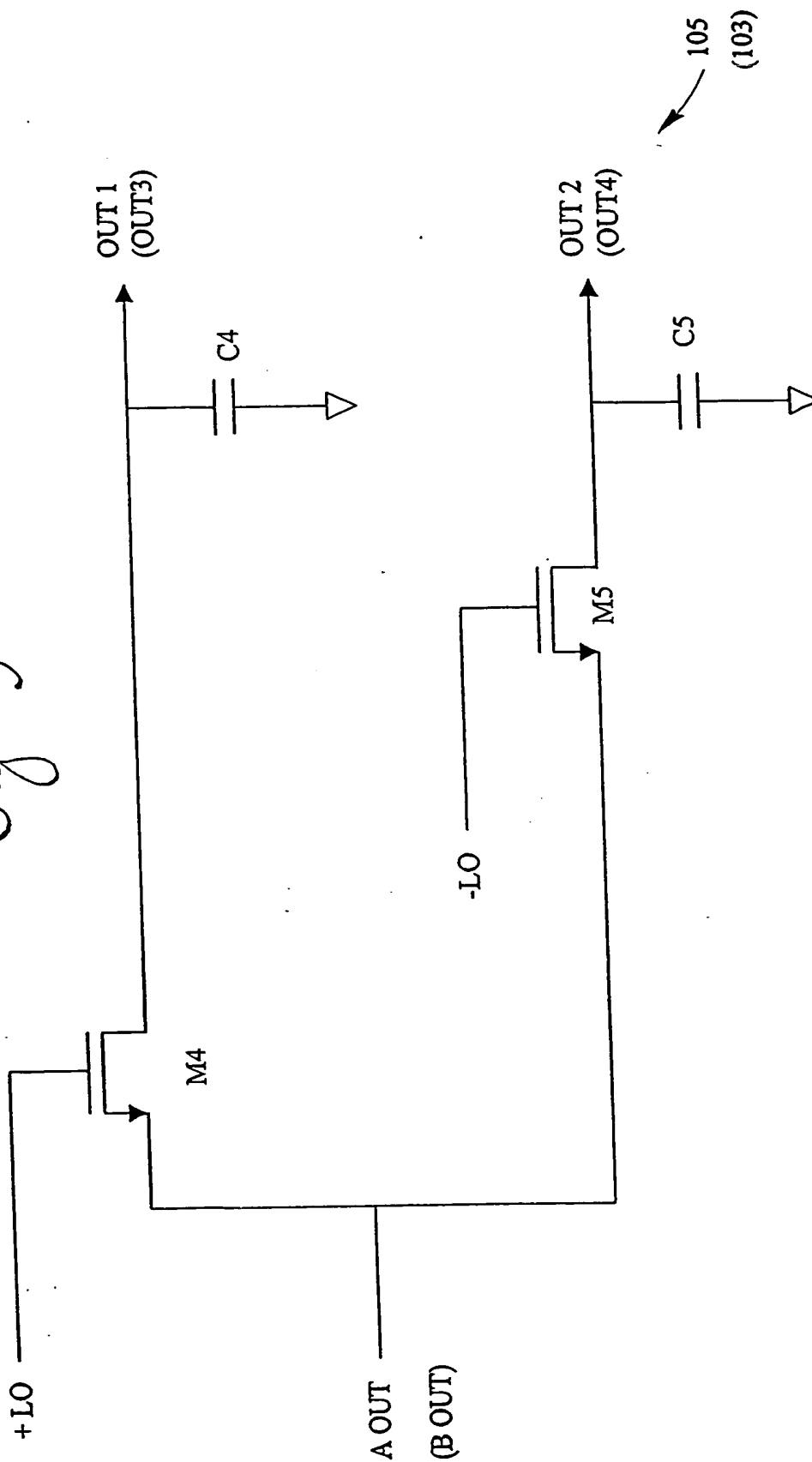


Fig. 30k

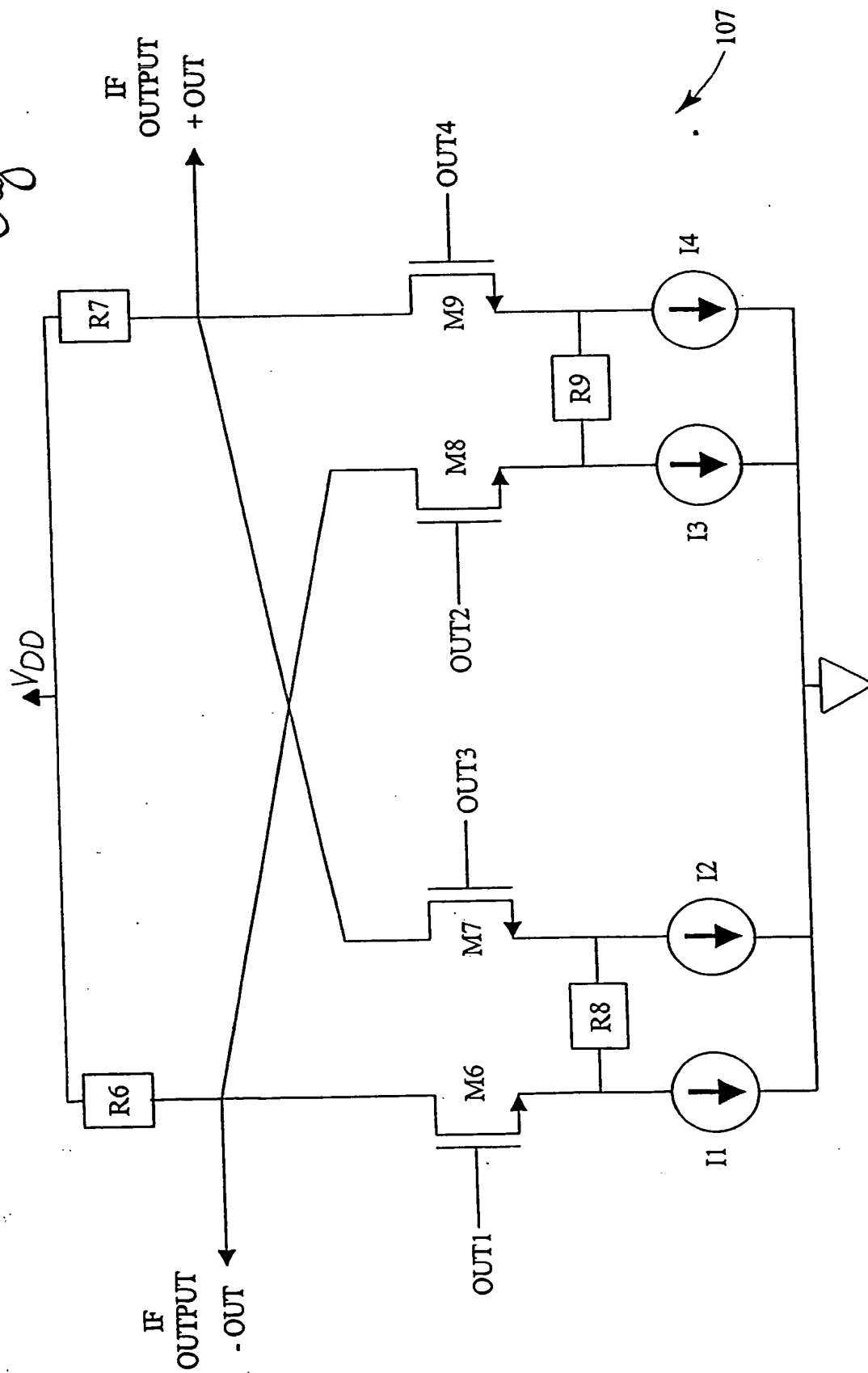
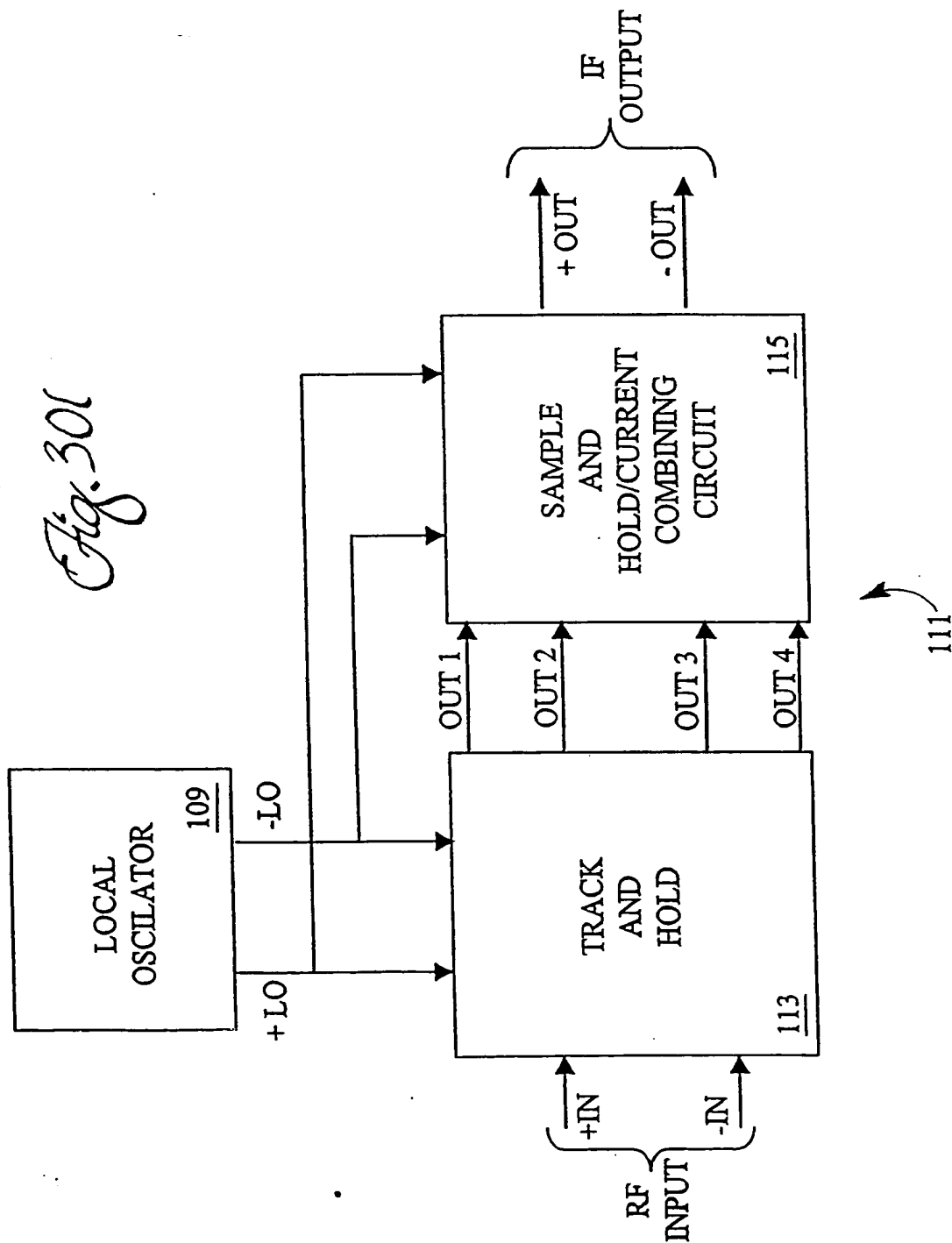




Fig. 301



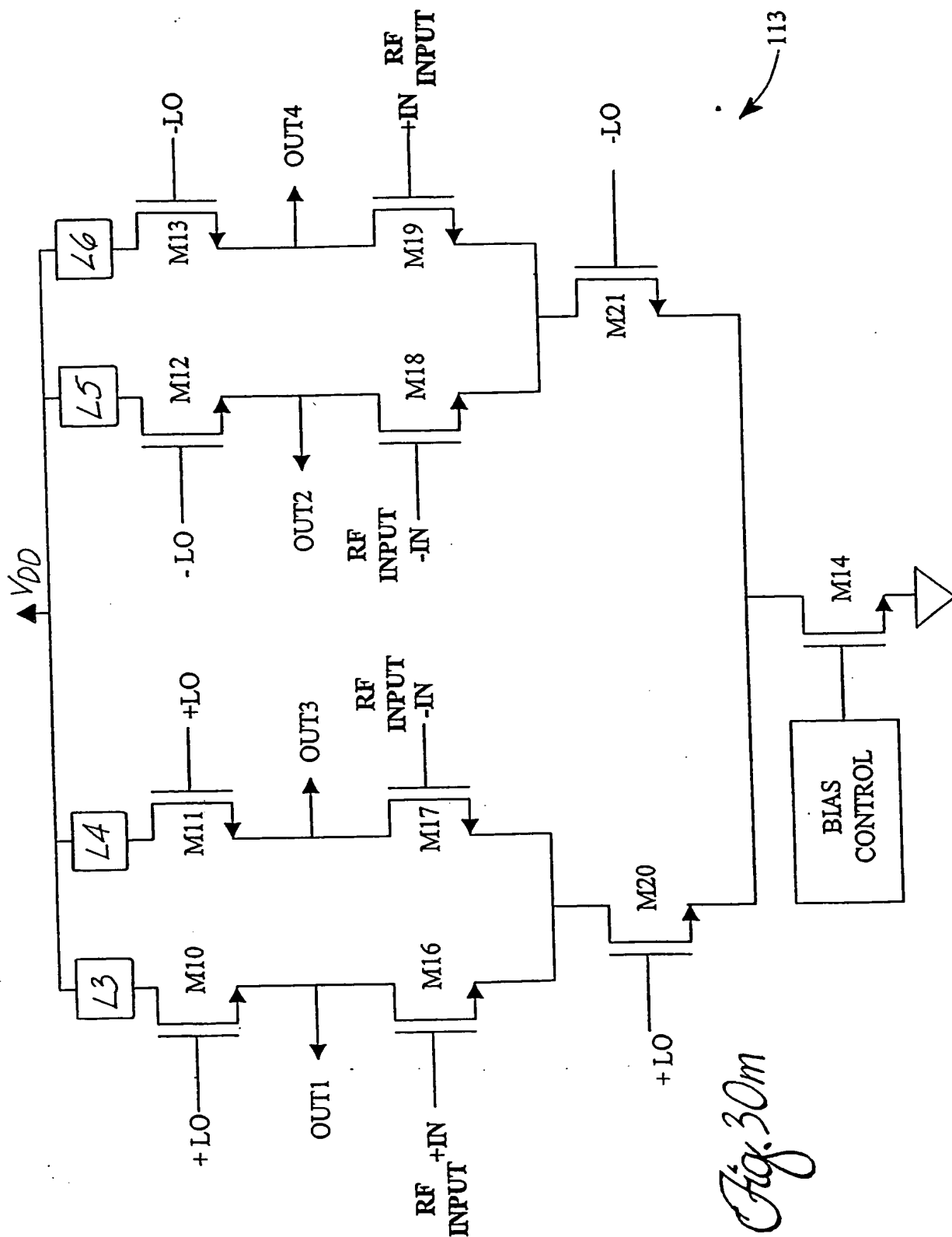


Fig. 30m

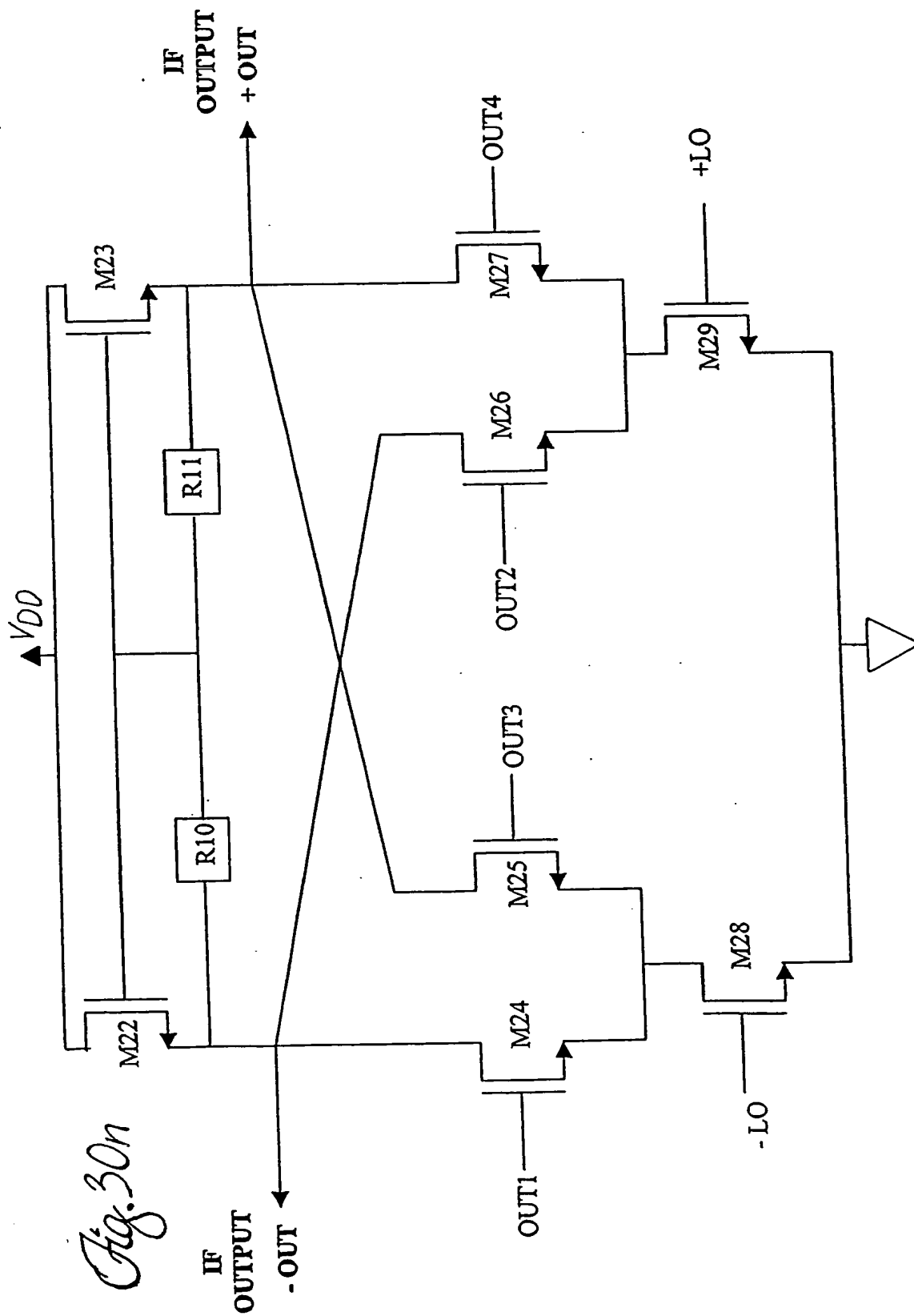


Fig. 30n

FIG. 31a

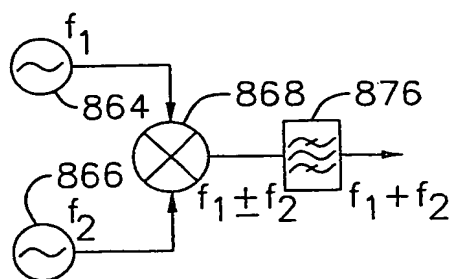


FIG. 31b

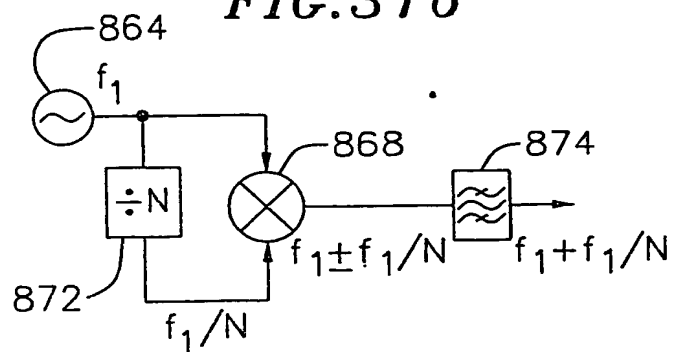


FIG. 32

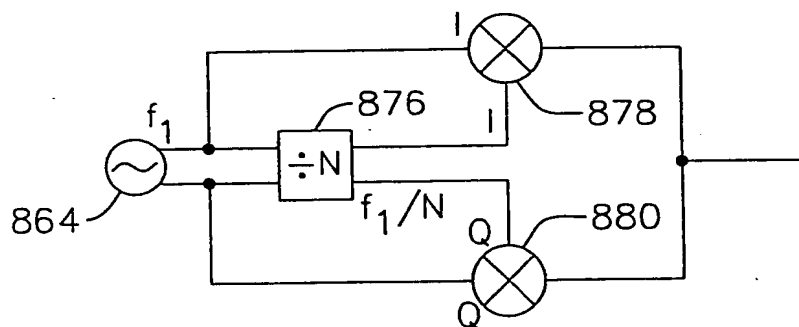


FIG. 33

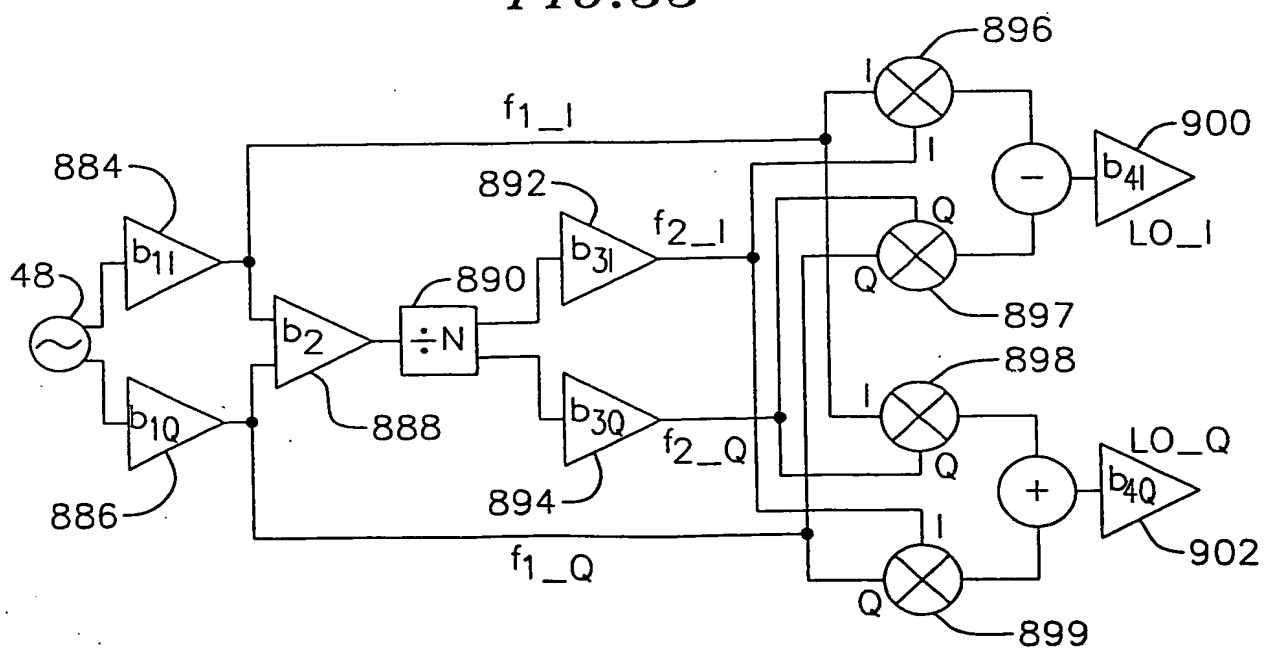


FIG. 33b

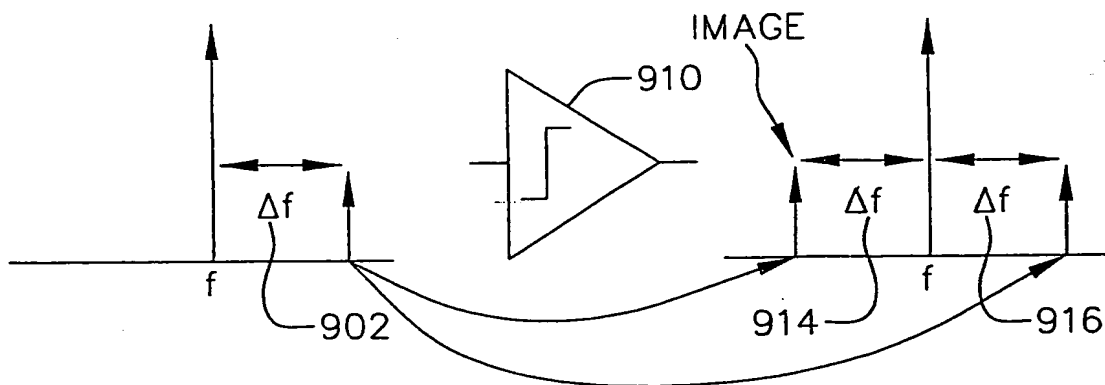


FIG. 34

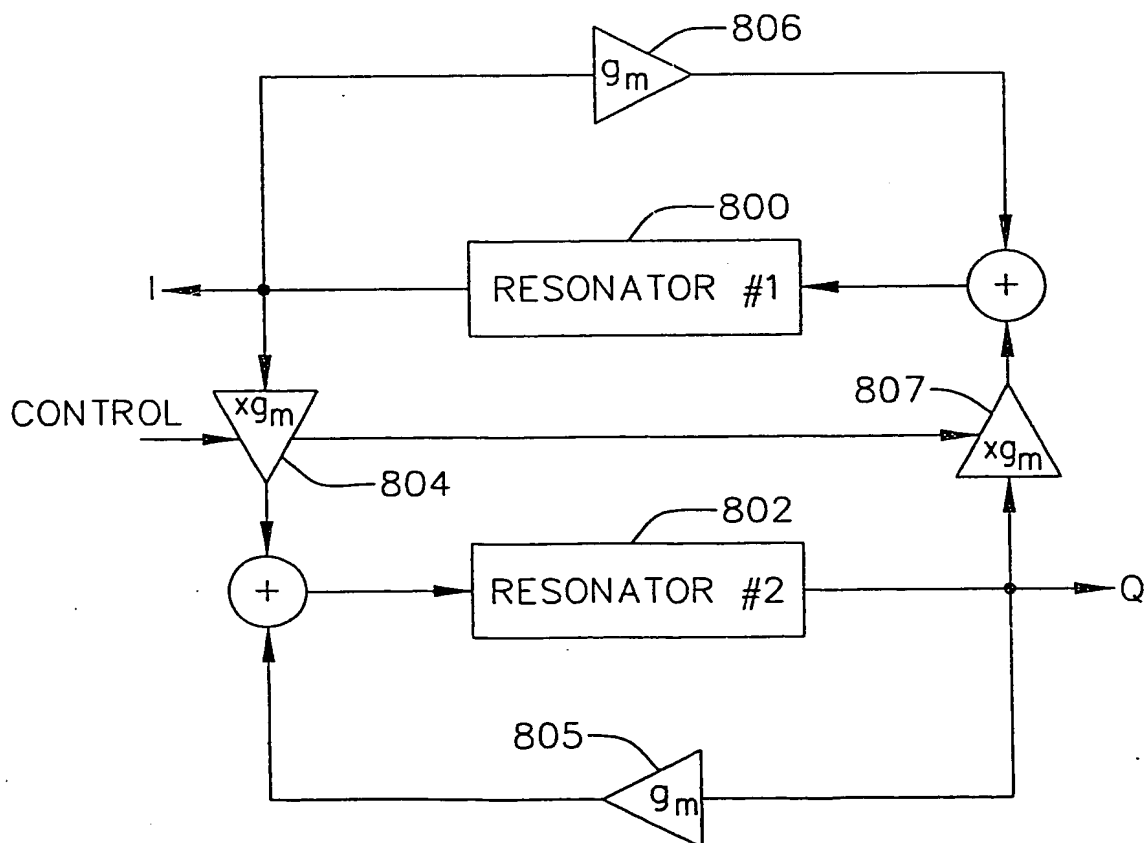
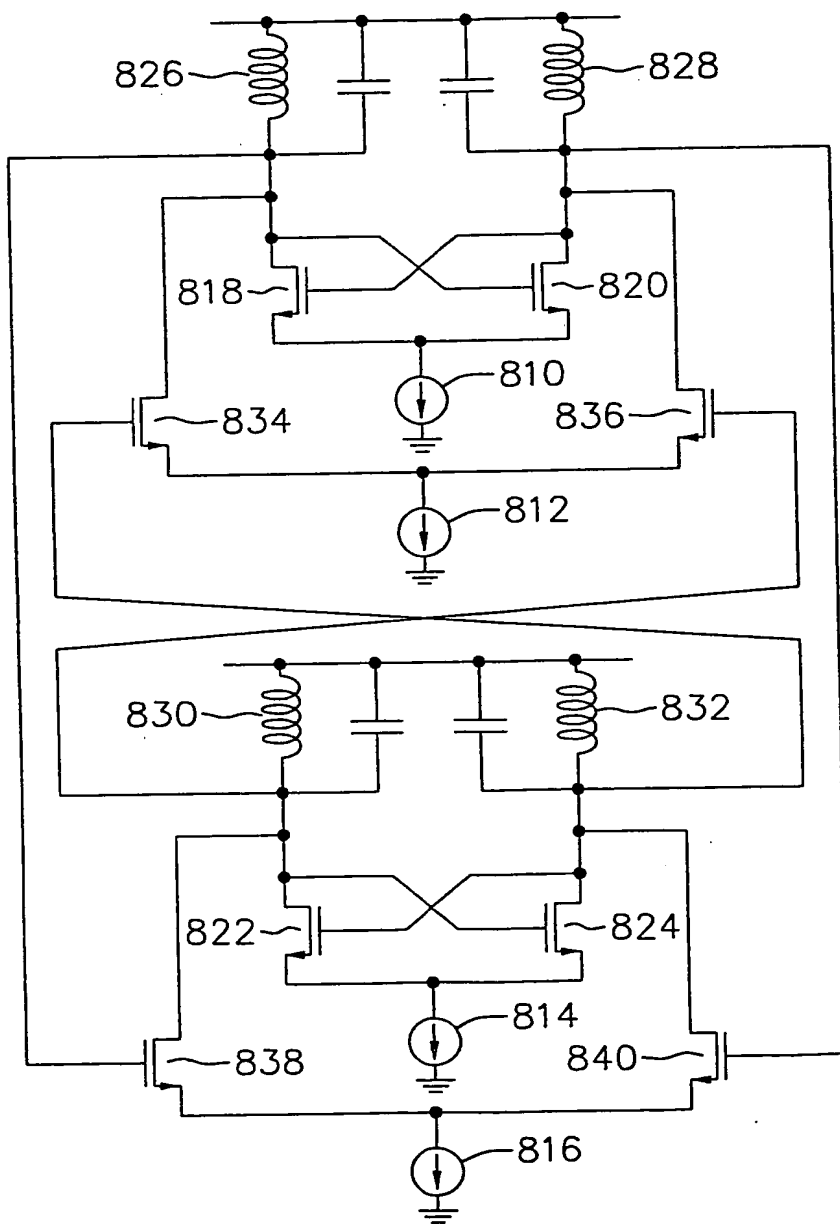


FIG. 35



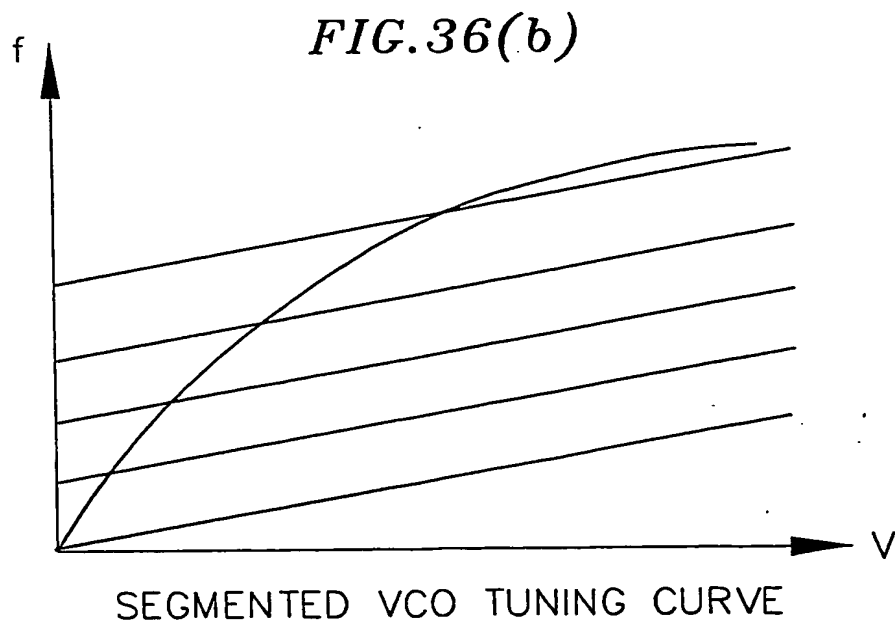
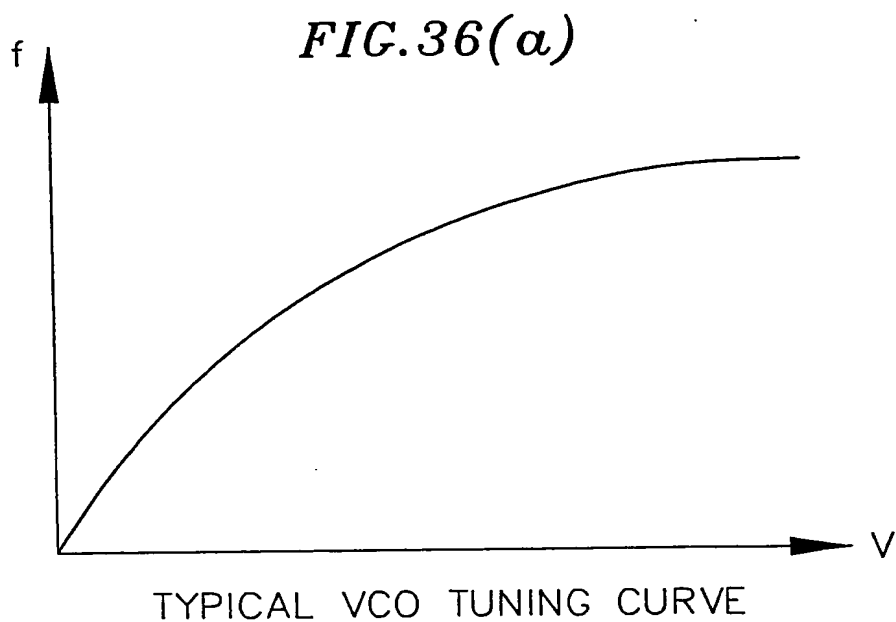


FIG. 37a

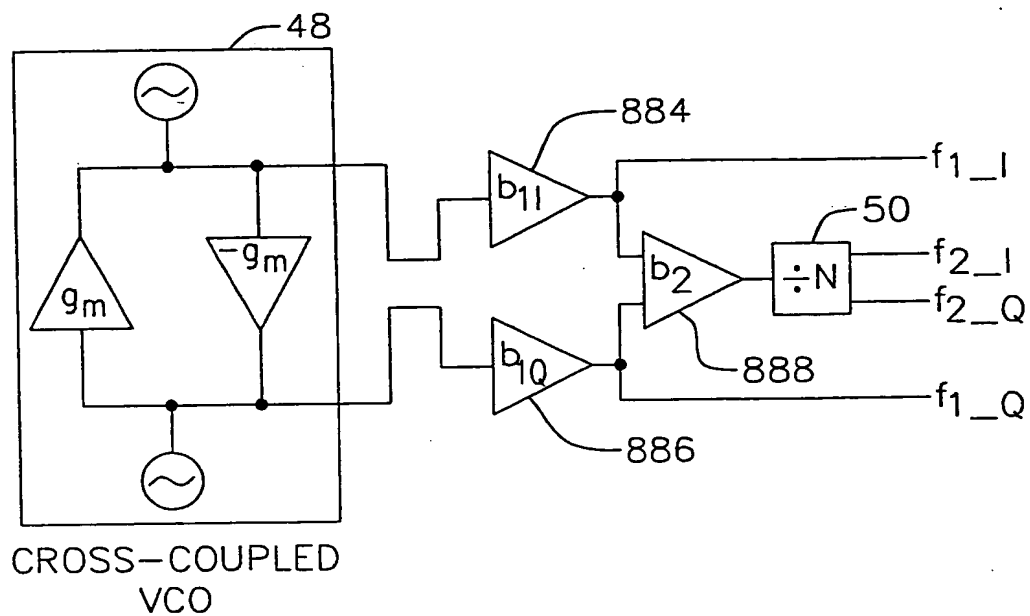
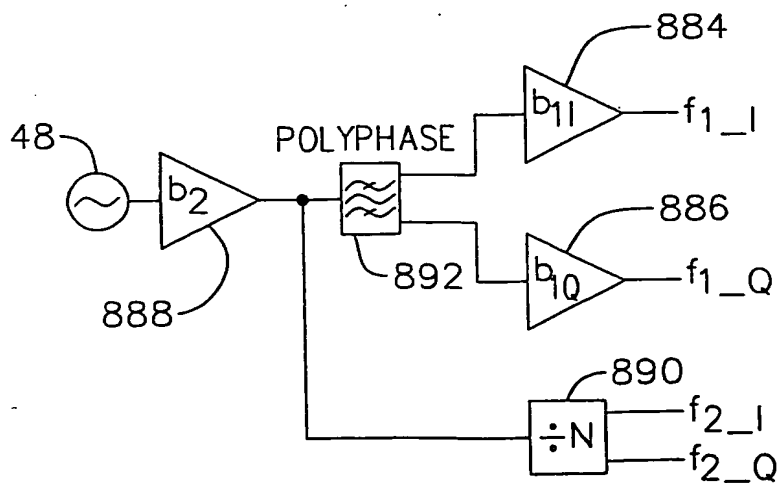
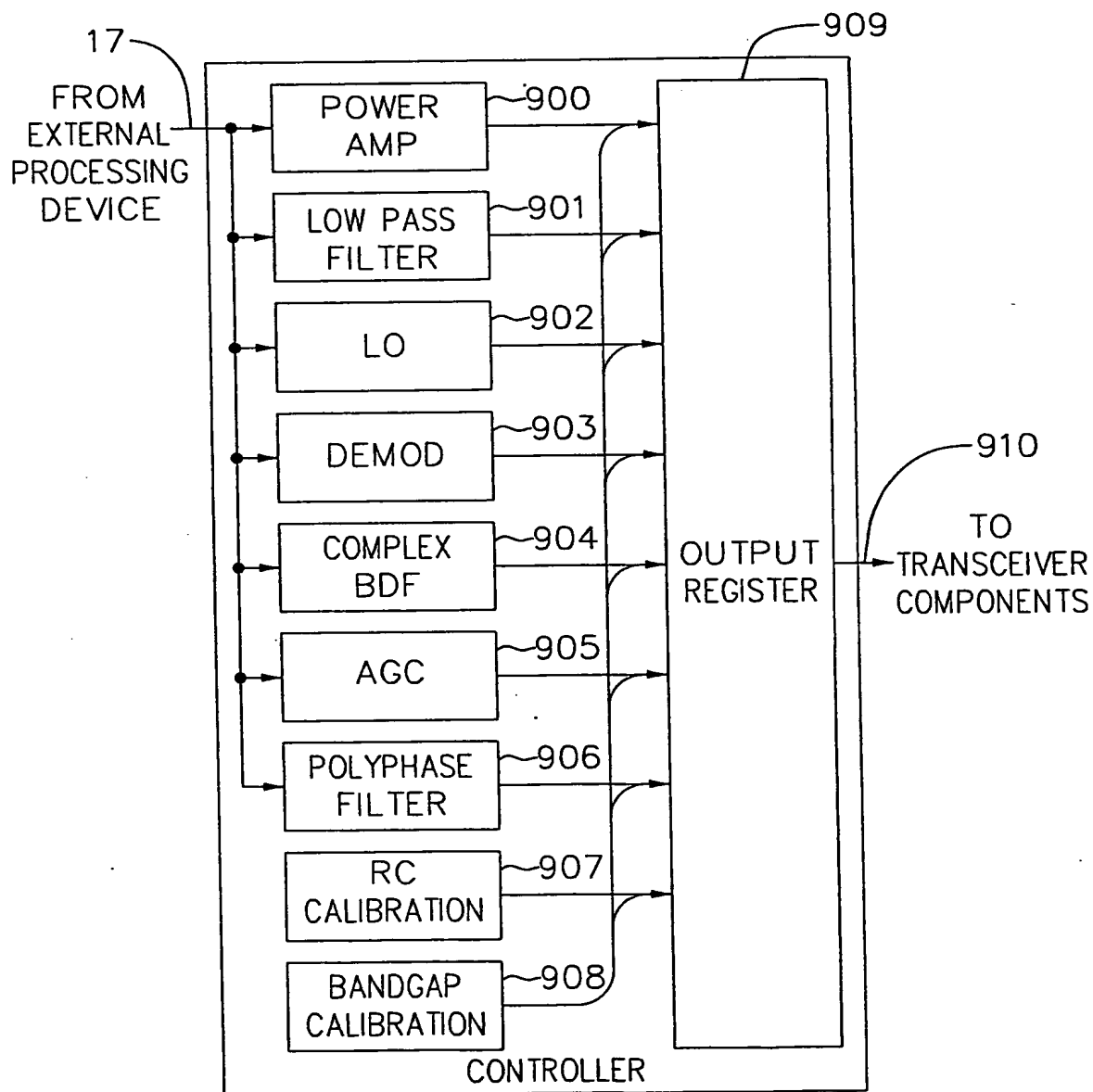


FIG. 37b



*FIG.38*

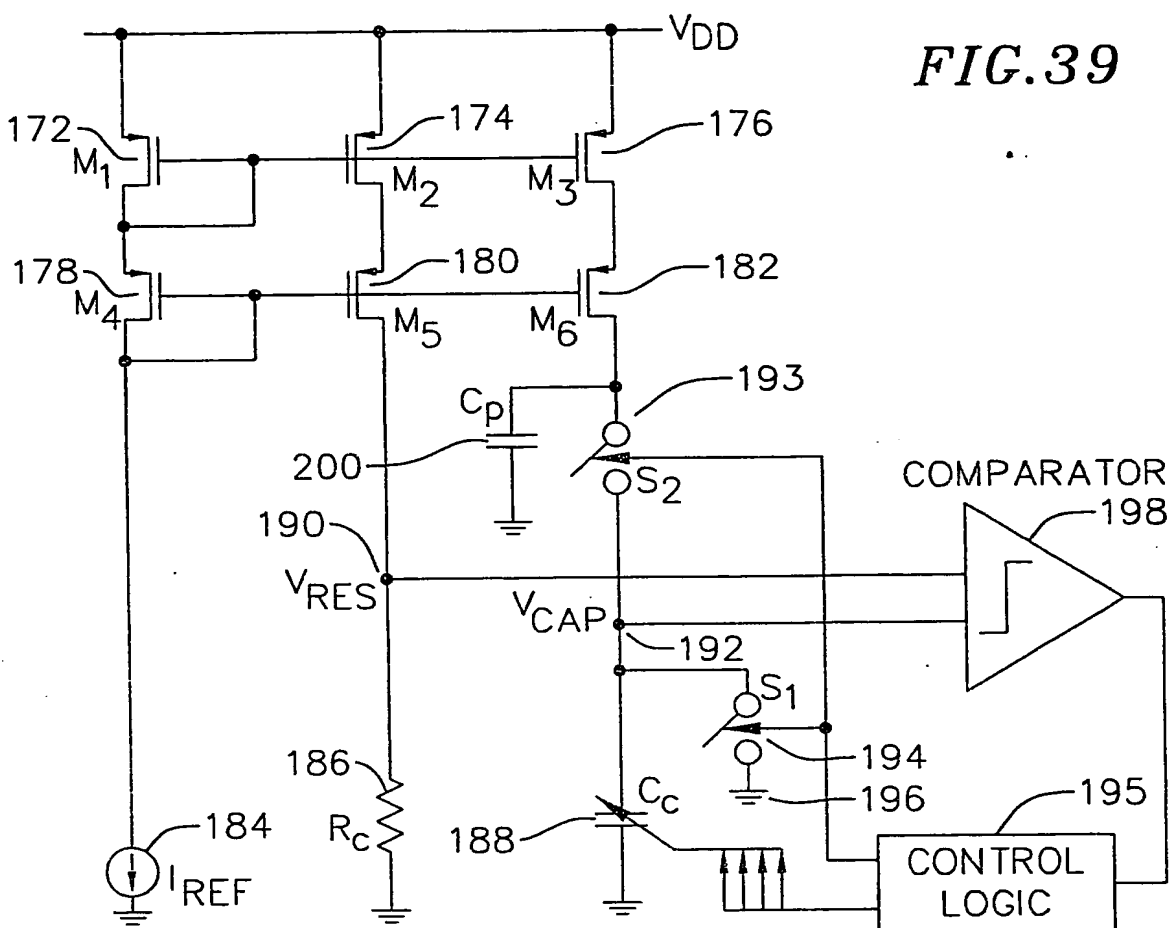
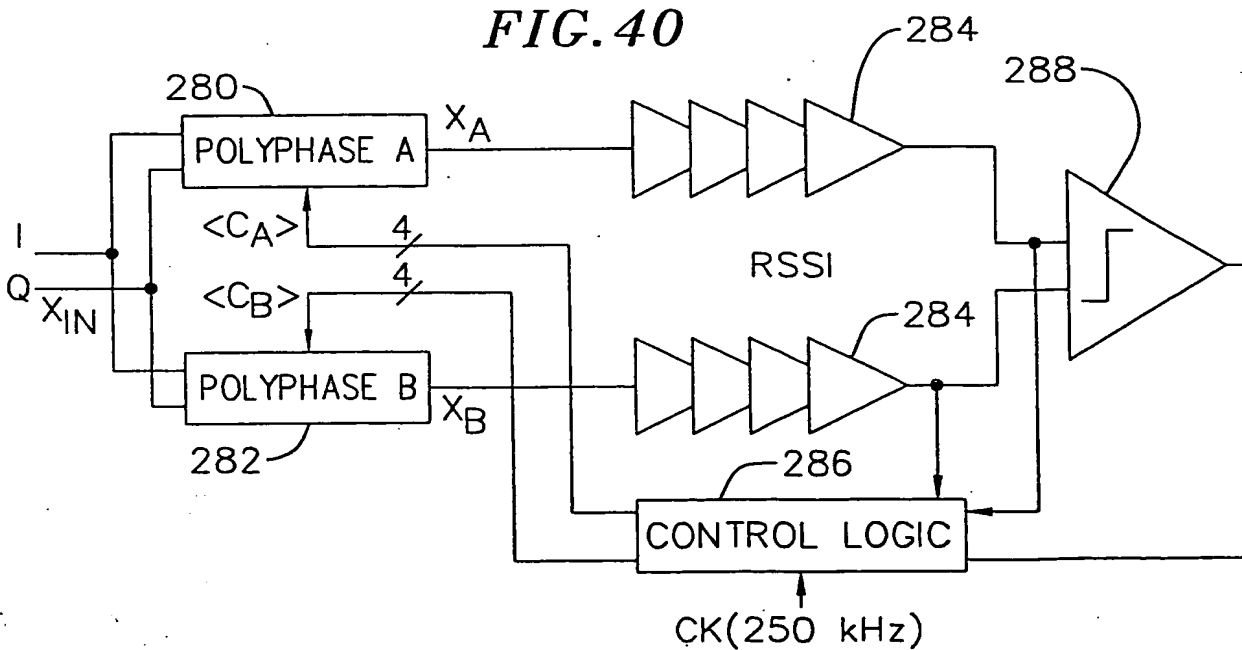


FIG. 40



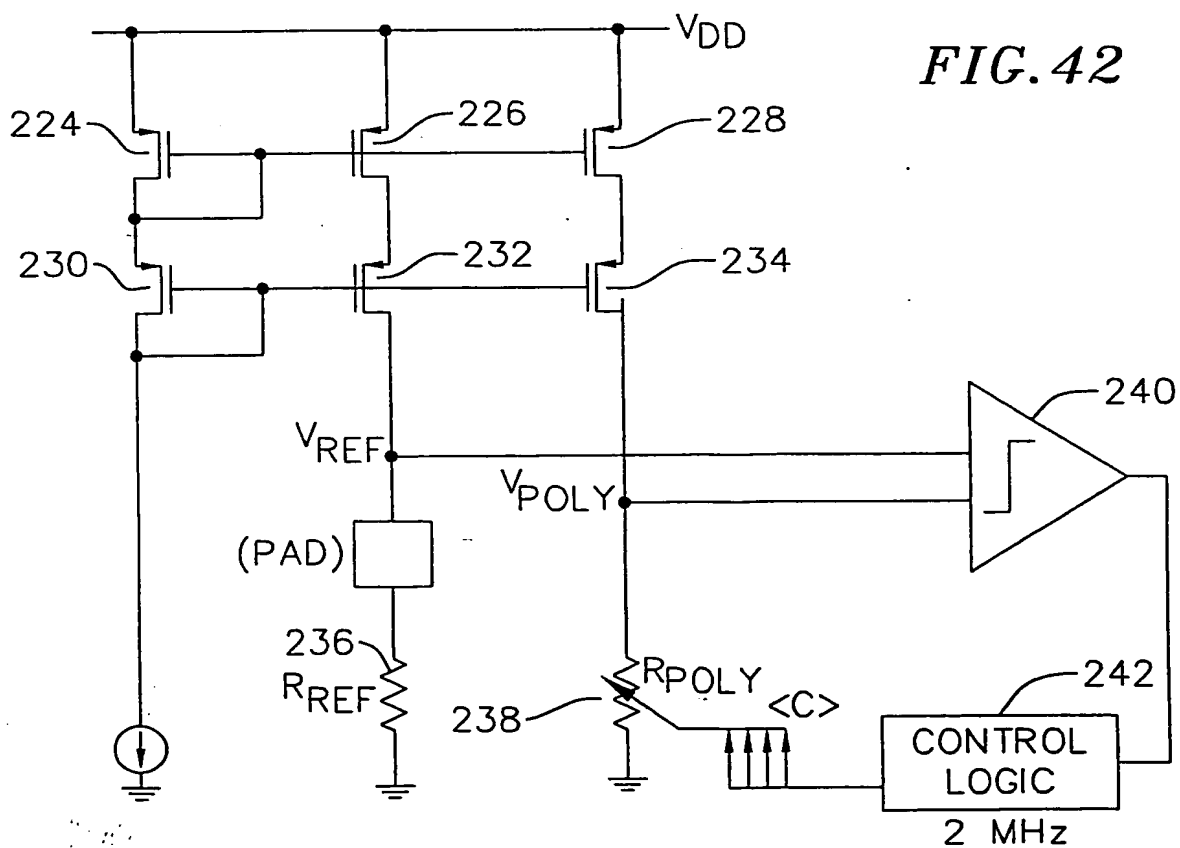
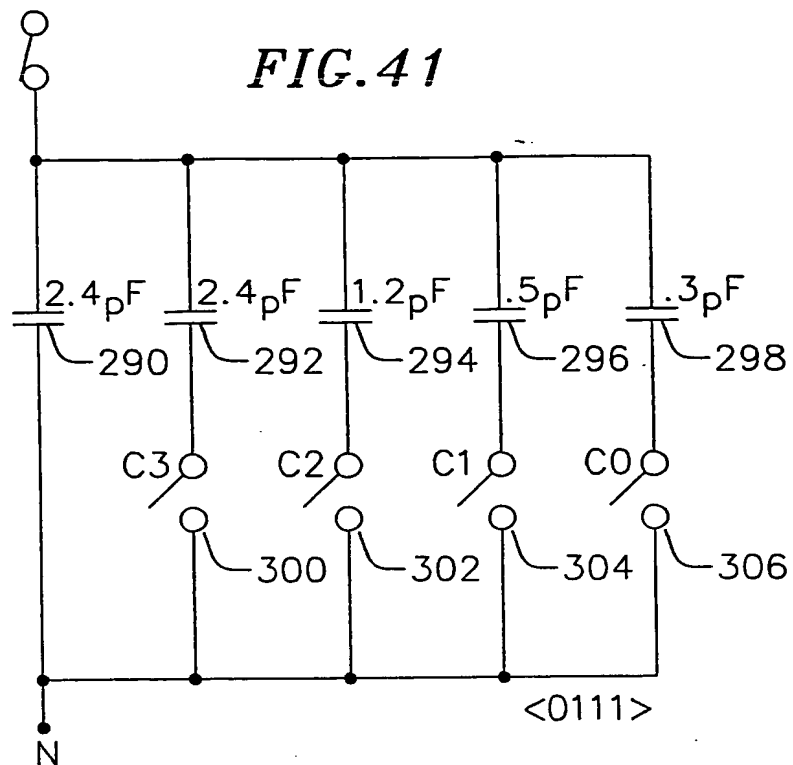


FIG. 43

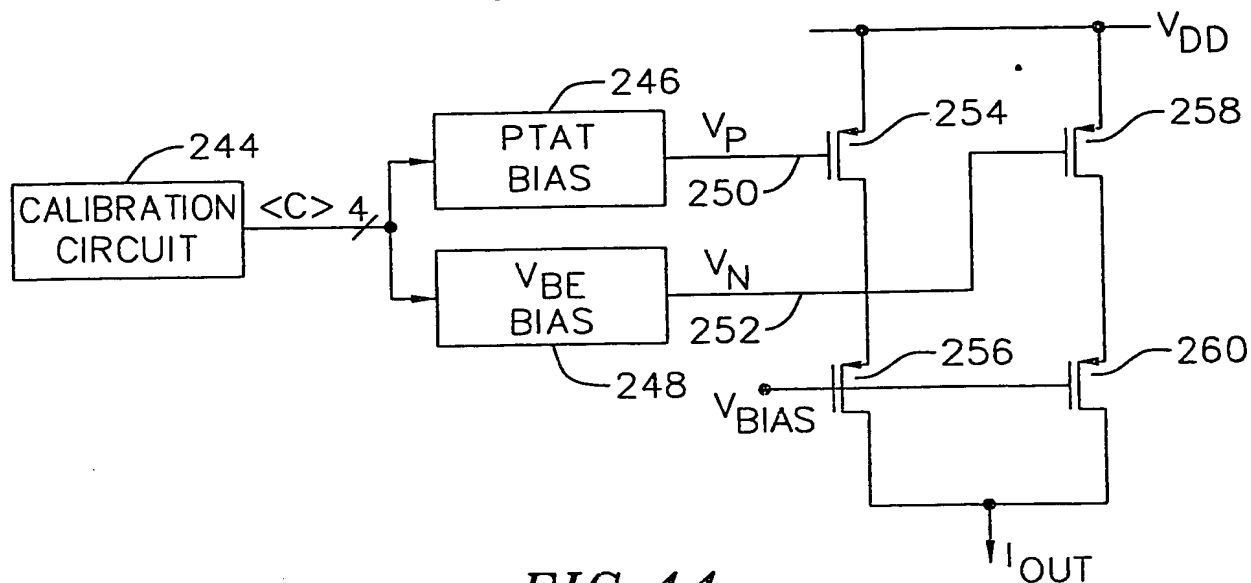


FIG. 44

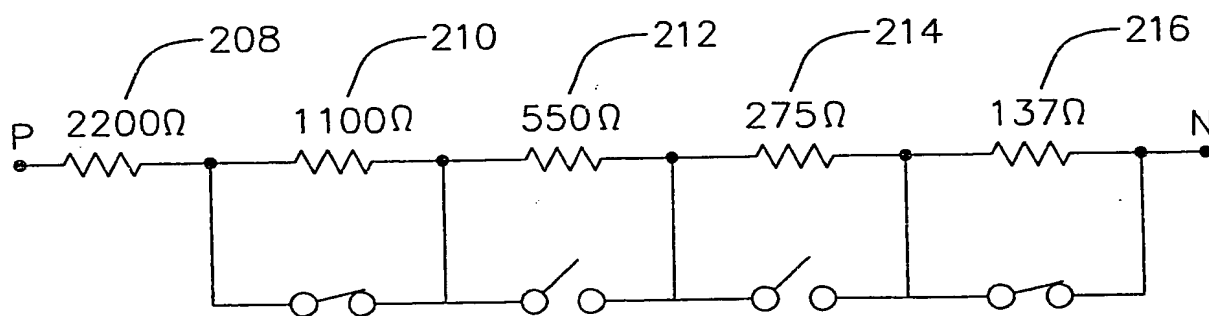
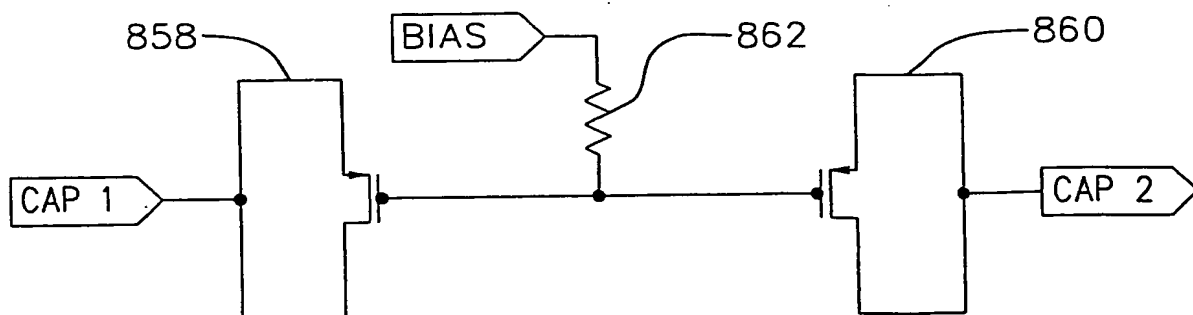


FIG. 45



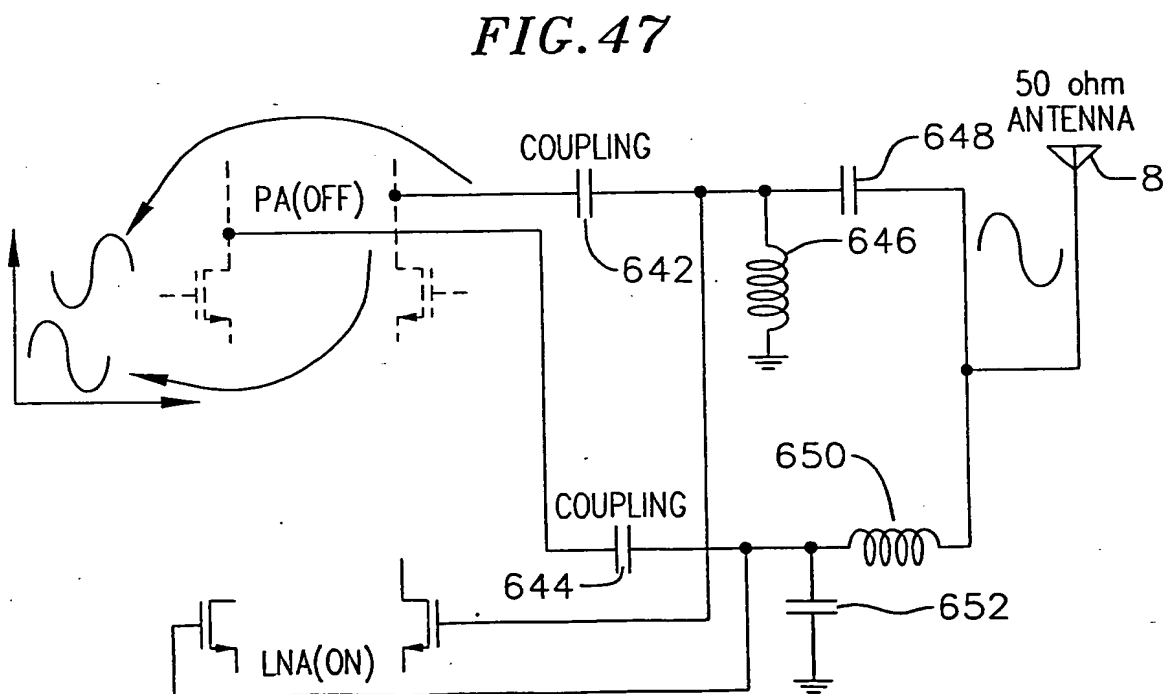
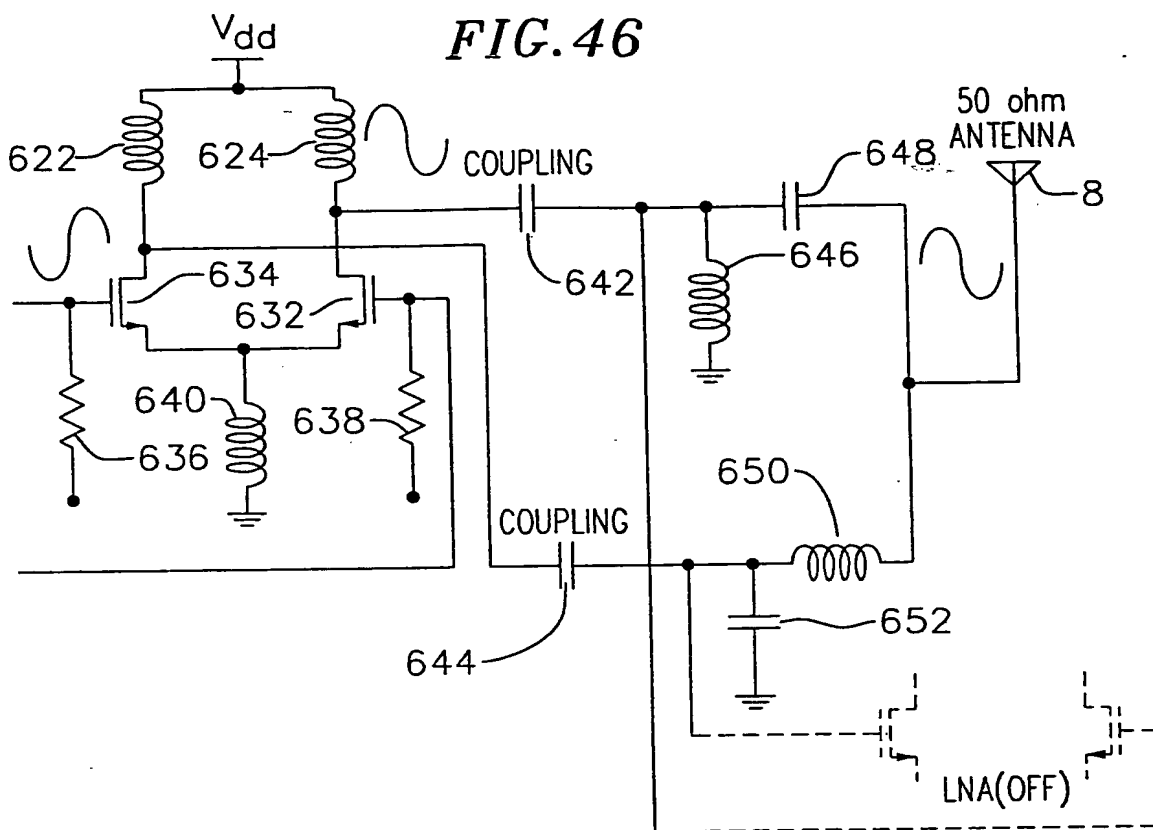
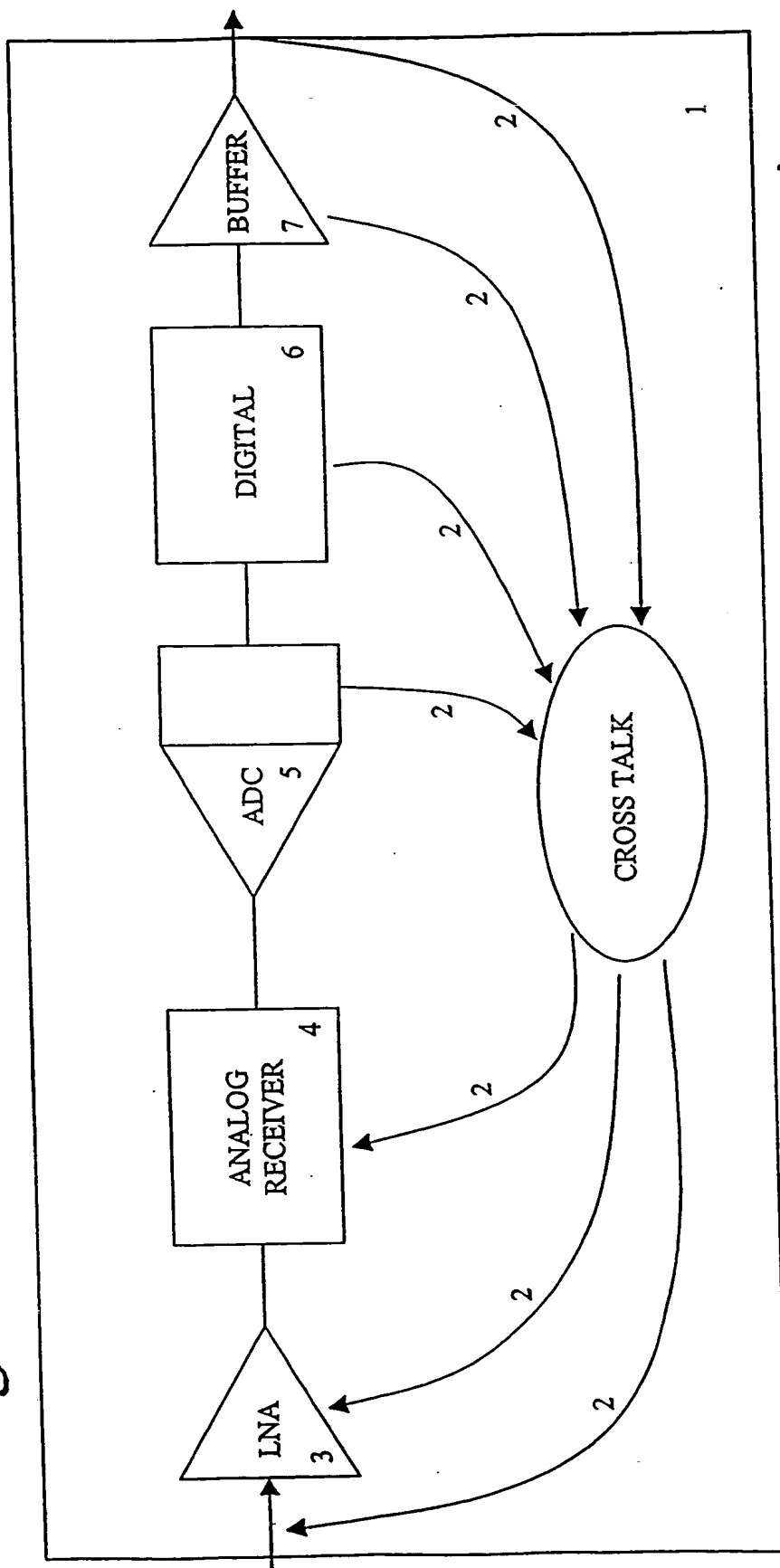
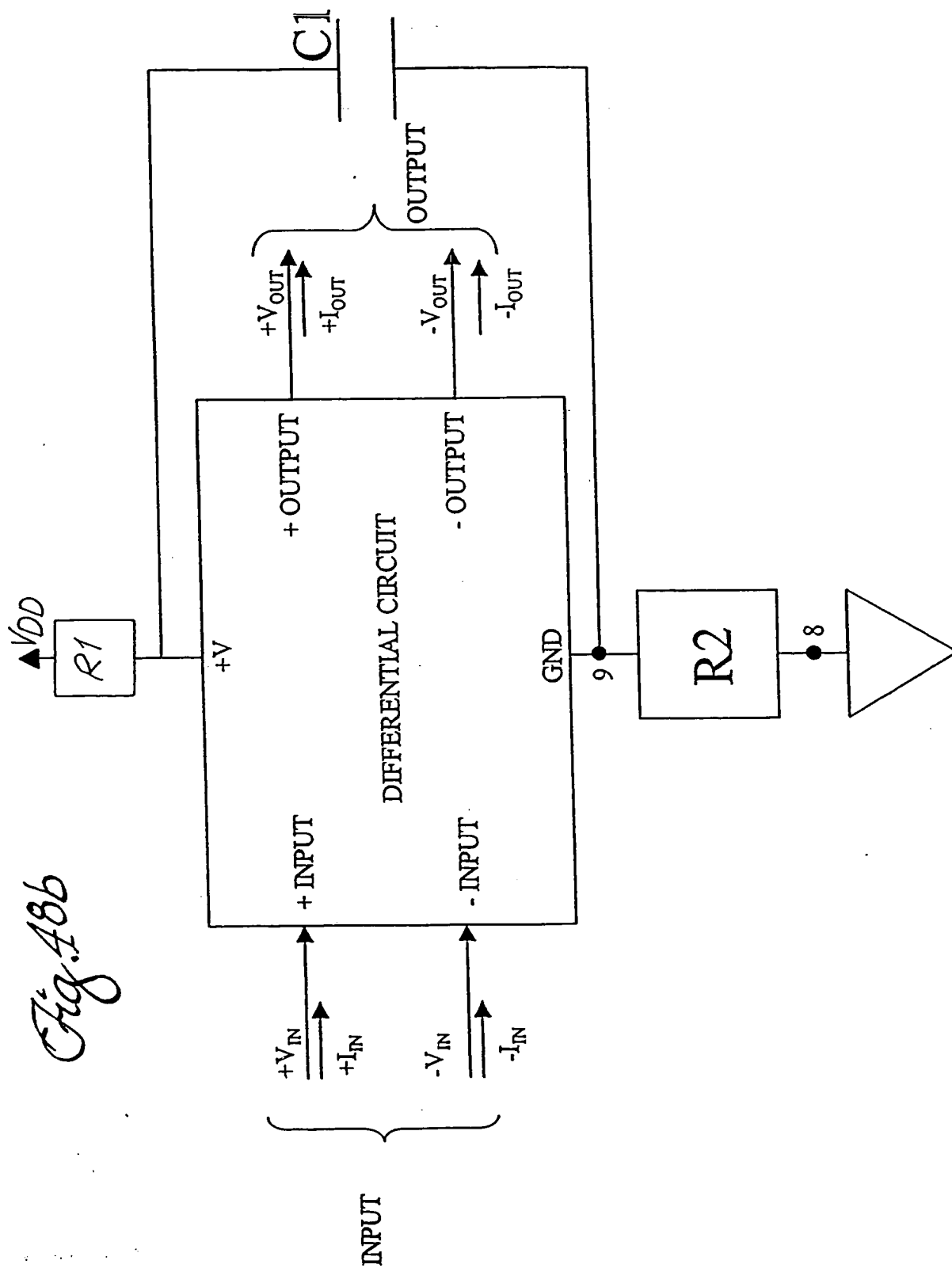
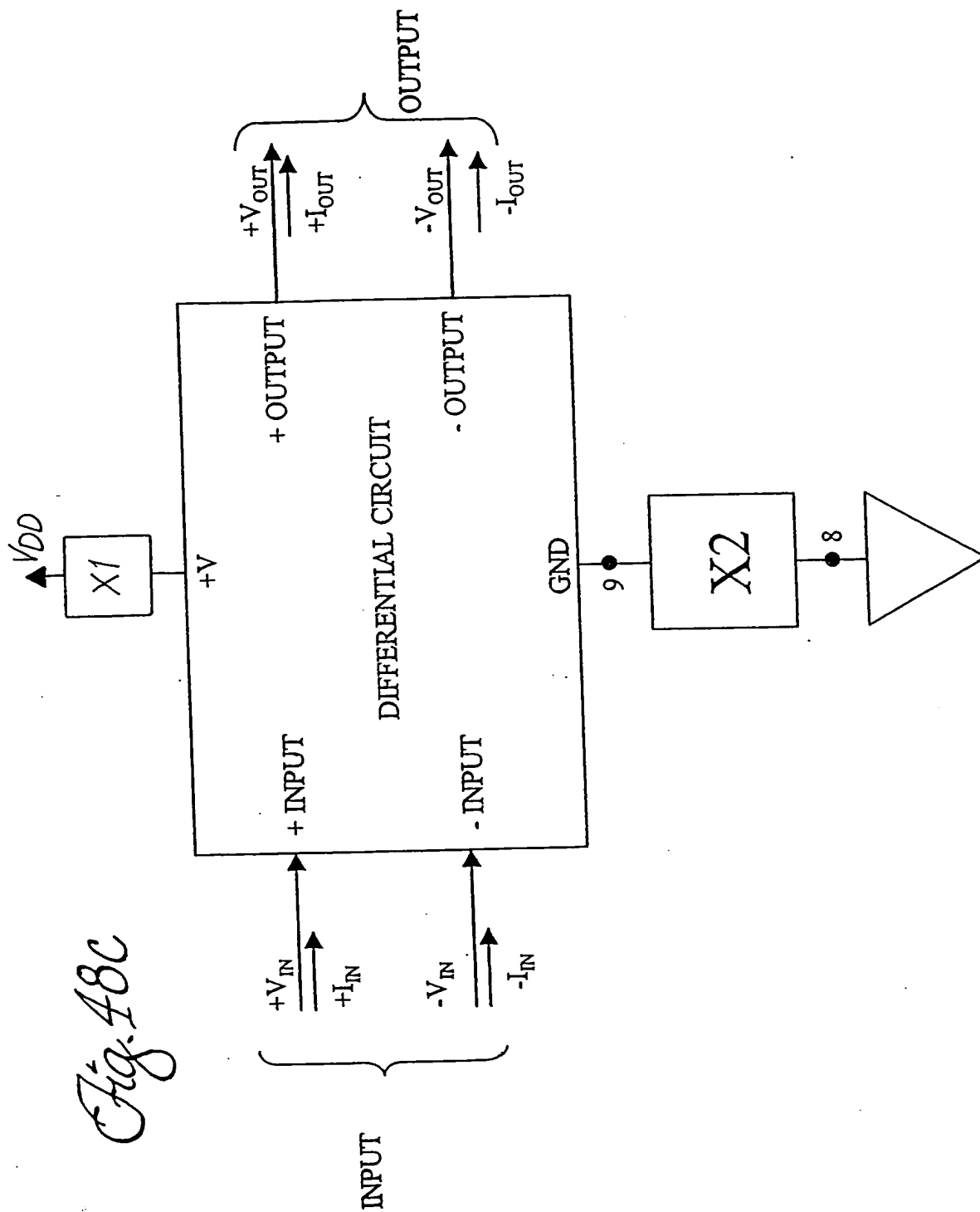


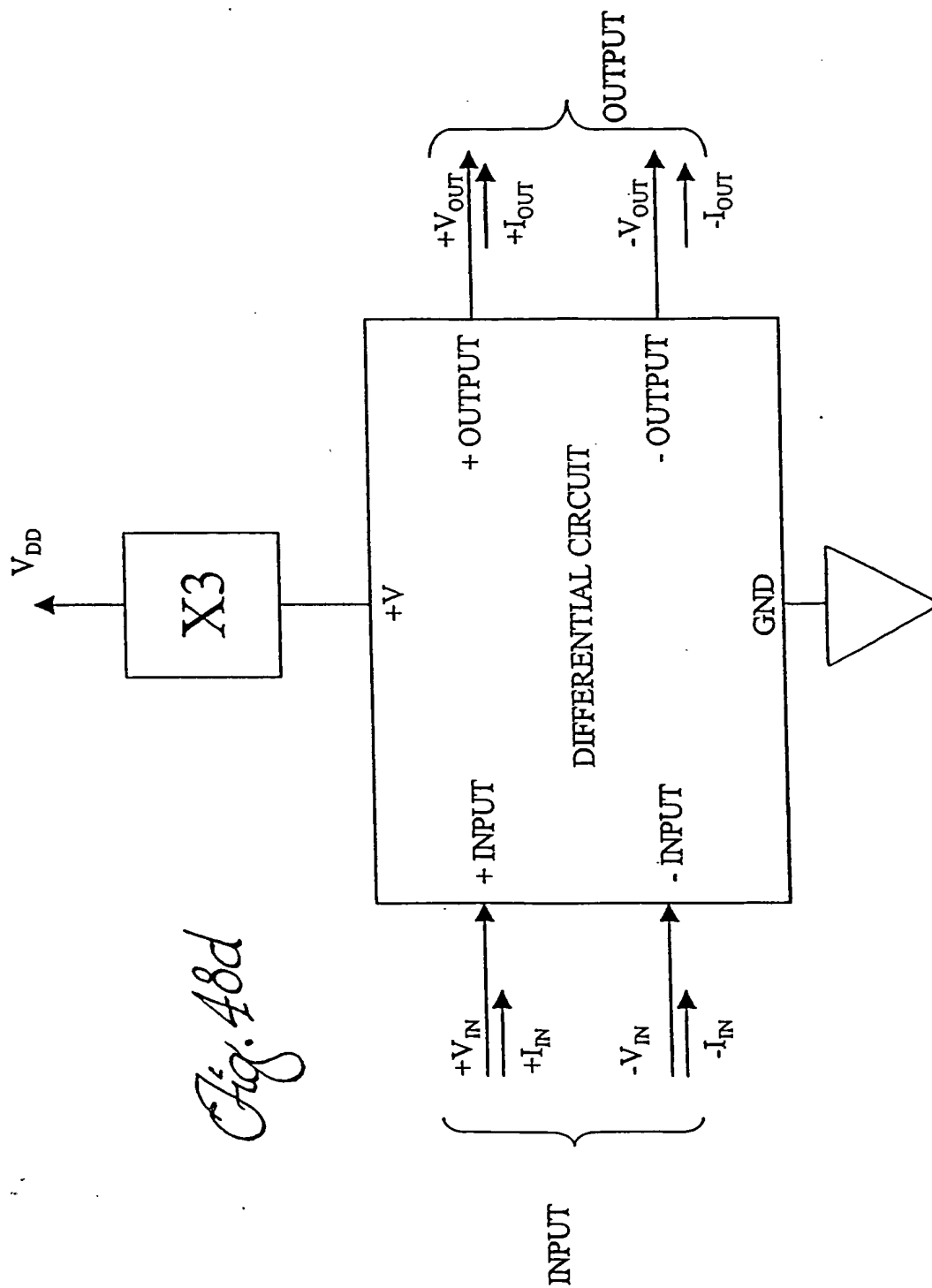


Fig. 48a









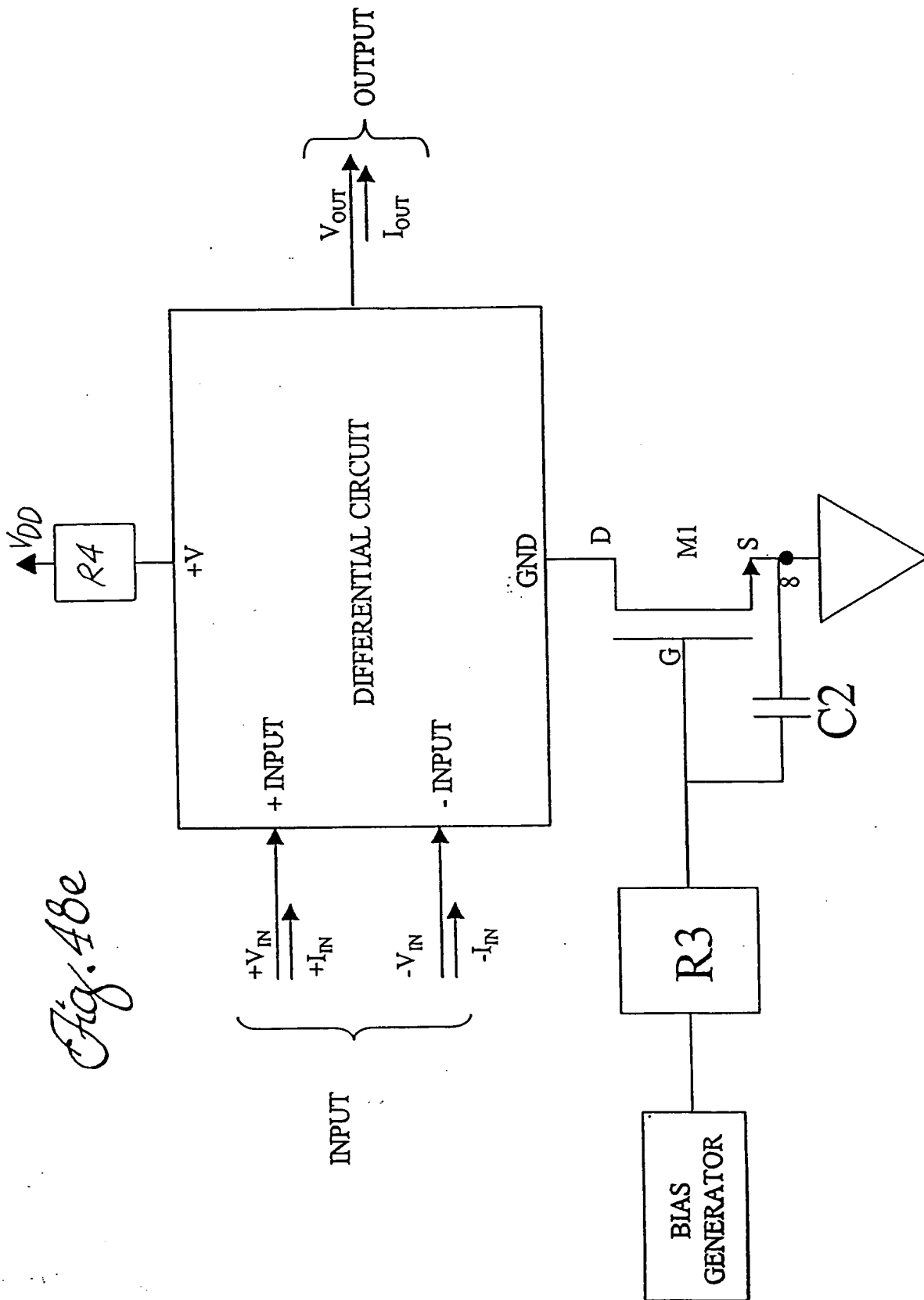


Fig. 48e

